REVISED HISTORY

DATE	ISSUE	CONTENTS OF CHANGES	S/W VERSION
APRIL/2003	ISSUE 1	Initial Release	S/W VERSION

The information in this manual is subject to change without notice and should not be construed as a commitment by LGE Inc. Furthermore, LGE Inc. reserves the right, without notice, to make changes to equipment design as advances in engineering and manufacturing methods warrant.

This manual provides the information necessary to install, program, operate and maintain the G7030

Table Of Contents

1. INTRODUCTION

1.1 Purpose

This manual provides the information necessary to repair, calibration, description and download the features of this model.

1.2 Regulatory Information

A. Security

Toll fraud, the unauthorized use of telecommunications system by an unauthorized part (for example, persons other than your company's employees, agents, subcontractors, or person working on your company's behalf) can result in substantial additional charges you're your telecommunications services. System users are responsible for the security of own system. There are may be risks of toll fraud associated with your telecommunications system. System users are responsible for programming and configuring the equipment to prevent unauthorized use. LGE does not warrant that this product is immune from the above case but will prevent unauthorized use of common-carrier telecommunication service of facilities accessed through or connected to it. LGE will not be responsible for any charges that result from such unauthorized use.

B. Incidence of Harm

If a telephone company determines that the equipment provided to customer is faulty and possibly causing harm or interruption in service to the telephone network, it should disconnect telephone service until repair can be done. A telephone company may temporarily disconnect service as long as repair is not done.

C. Changes in Service

A local telephone company may make changes in its communications facilities or procedure. If these changes could reasonably be expected to affect the use of the G7030 or compatibility with the network, the telephone company is required to give advanced written notice to the user, allowing the user to take appropriate steps to maintain telephone service.

D. Maintenance Limitations

Maintenance limitations on the G7030 must be performed only by the LGE or its authorized agent. The user may not make any changes and/or repairs expect as specifically noted in this manual. Theref ore, note that unauthorized alternations or repair may affect the regulatory status of the system and may void any remaining warranty.

E. Notice of Radiated Emissions

The G7030 complies with rules regarding radiation and radio frequency emission as defined by local regulatory agencies. In accordance with these agencies, you may be required to provide information such as the following to the end user.

F. Pictures

The pictures in this manual are for illustrative purposes only; your actual hardware may look slightly different.

G. Interference and Attenuation

An G7030 may interfere with sensitive laboratory equipment, medical equipment, etc. Interference from unsuppressed engines or electric motors may cause problems.

H. Electrostatic Sensitive Devices

ATTENTION

Boards, which contain Electrostatic Sensitive Device (ESD), are indicated by the  sign.
Following information is ESD handling:

- Service personnel should ground themselves by using a wrist strap when exchange system boards.
- When repairs are made to a system board, they should spread the floor with anti-static mat which is also grounded.
- Use a suitable, grounded soldering iron.
- Keep sensitive parts in these protective packages until these are used.
- When returning system boards or parts like EEPROM to the factory, use the protective package as described.

1.3 Abbreviations

For the purposes of this manual, following abbreviations apply:

APC	Automatic Power Control
BB	Baseband
BER	Bit Error Ratio
CC-CV	Constant Current – Constant Voltage
DAC	Digital to Analog Converter
DCS	Digital Communication System
dBm	dB relative to 1 milliwatt
DSP	Digital Signal Processing
EEPROM	Electrical Erasable Programmable Read-Only Memory
EL	Electroluminescence
ESD	Electrostatic Discharge
FPCB	Flexible Printed Circuit Board
GMSK	Gaussian Minimum Shift Keying
GPIB	General Purpose Interface Bus
GSM	Global System for Mobile Communications
IPUI	International Portable User Identity
IF	Intermediate Frequency
LCD	Liquid Crystal Display
LDO	Low Drop Output
LED	Light Emitting Diode
OPLL	Offset Phase Locked Loop
PAM	Power Amplifier Module
PCB	Printed Circuit Board
PGA	Programmable Gain Amplifier
PLL	Phase Locked Loop
PSTN	Public Switched Telephone Network
RF	Radio Frequency
RLR	Receiving Loudness Rating
RMS	Root Mean Square
RTC	Real Time Clock
SAW	Surface Acoustic Wave
SIM	Subscriber Identity Module
SLR	Sending Loudness Rating
SRAM	Static Random Access Memory
STMR	Side Tone Masking Rating
TA	Travel Adapter
TDD	Time Division Duplex
TDMA	Time Division Multiple Access
UART	Universal Asynchronous Receiver/Transmitter
VCO	Voltage Controlled Oscillator
VCTCXO	Voltage Control Temperature Compensated Crystal Oscillator
WAP	Wireless Application Protocol

2. PERFORMANCE

2.1 Product Name

G7030: Support GPRS(Class 10)

2.2 Supporting Standard

Item	Feature	Comment
Supporting Standard	E-GSM/ DCS Dual Band with seamless handover Phase 2+ SIM Toolkit : Class 1,2,3	
Frequency Range	E-GSM TX : 880 – 915 MHz E-GSM RX : 925 – 960 MHz DCS 1800 TX : 1710 – 1785 MHz DCS 1800 RX : 1805 – 1880 MHz	
Application Standard	WAP 1.2.1 : Yes IrDA 1.2	

2.3 Main Parts : GSM Solution

	G7030
Digital Baseband	Hercrom400G2 Rev.B @39MHz (XF741979-BGHH)
Analog Baseband	Nausica_CS Rev.2.1 (PTWLR3012BGGM)
RF Chip	Aero (Multi slot) (Si4200-BM, Si4201-BM, Si4133T-BM)

2.4 H/W Features

Item	Feature	Comment
Form Factor	Flip Type(Folder)	Dual LCD (65k&256 Color)
Battery	1) Capacity Standard : Li-Ion, 740mAh	Cell Size : Standard 50(L) x 34(W) x 46(H)mm
	2) Packing Type : Hard Pack	
Size	Standard : 87(L) x 45(W) x 25(H)mm	
Weight	89g	With Battery
PCB	One PCB:8 Layers, 1t	

2.4 H/W Features

Item	Feature	Comment
AVG current(mA)	Max : 150mA (Power Level 19) Max : 320mA (Power Level 5)	Estimated
Standby Current	Max : 4.0mA @ *Paging Period 9	Estimated
Stand by time	Up to 180 hours @ Paging Period: 9	@ 740mAh
Charging time	Below 2.5 hr.	@ Power Off / 740mAh
Talk time	Min : 2hr30min @GSM Power Level 7 Min : 4hr30min @GSM Power Level 12	@ 740mAh
RX sensitivity	GSM 900 : -107 dBm DCS 1800 : -107 dBm	
TX output power	GSM 900 : 32 dBm DCS 1800 : 29 dBm	Class4 (GSM) Class1 (DCS)
GPRS compatibility	*GPRS Class 10	
SIM card type	Plug-In SIM 3V / 5V	
Display	**1. Main LCD** **2. 65K Color-STN (128 X160)** Pixels : (0.219 x 0.219) mm View Area : (30.54 x 36.04) mm Active Area : (28.02 x 35.028) mm Backlight : White LED **3. Sub LCD** **4. 256 Color : OELD (96 x 64)** Pixels : (0.219 x 0.251) mm View Area :(23.16 x 18.12) mm Active Area :(20.997 x 16.04) mm	
Status Indicator	N/A	
Keypad	Alphanumeric Key : 12 Function Key : 12 Side Key : 2 Total # of Keys : 26	Function Key: 4 Key Navigation, OK, F1, F2, SND, END/PWR, Clear, Book Mark, Voice Recording
ANT	Fixed Type	
System connector	24 Pin	
Ear Phone Jack	3 Pole (ϕ2.5mm)	
PC synchronization	Yes	
Memory	Flash : 128Mbit SRAM : 32Mbit	Toshiba
Speech coding	FR, EFR, HR	

Item	Feature	Comment
Data & Fax	Built in Data & Fax support	
Vibrator	Built in Vibrator	
IrDA	Built in IrDA	PC sync support
MIDI (for Buzzer Function)	40 Poly	Buzzer Function By Using MIDI IC
Voice Recording	up to 90 sec	30sec x 3
Travel Adapter	Yes	
Options	Ear-Microphone Cigarette Lighter Adapter Data Cable Hands free Car Kit Simple Hands Free kit	 TBD TBD

*** Battery Capacity : 740mAh (at now)**

2.5 S/W Features

Item	Feature	Comment
RSSI	*0 ~ 5 Levels	
Battery Charging	*0 ~ 3 Levels	
Key Volume	0 ~ 5 Level	6dB per step
Audio Volume	1 ~ 5 Level	"
Time / Date Display	Yes	
Multi-Language	Yes	
Quick Access Mode	Phonebook / WAP / Profile	(WAP by OK long key)
PC Sync	Schedule / Phonebook / SMS	MS Scheduler & Outlook
Speed Dial	Yes (2~9)	Voice mail center → 1 key
Profile	Yes	Menu+3
***CLIP / CLIR**	Yes (different melody - Phone Book Gr.)	Names+3(Options+3)
Phonebook	3 Numbers + 1 Memo + 1 e-mail	Total 255 Members
Last Dial Number	Yes (20)	
Last Received Number	Yes (20)	
Last Missed Number	Yes (10)	
Search Number / Name	Yes	

Item	Feature	Comment
Group	7 / User Editor	Names+3
***Fixed Dial Number**	Yes	Menu+4+5+3
Voice Memo	30 secs * 3	
Call Remainder	Yes	
Network Selection	Automatic / Manual	Menu+4+6
Mute	Yes	
Call Divert	Yes	Menu+5
Call Barring	Yes	Menu+4+5+2
Call Charge	Yes	Menu+2+6
Call Duration	Yes	Menu+2+5
SMS (EMS)	100	
***EMS Send / Receive / Save**	Yes	Melody / Picture /Animation
WAP Browser	WAP 1.2.1	
Wall Paper	Yes	
Download Melody / Wallpaper (MMS)	Over the WAP	
Long Message	MAX 480 Characters(3page*160)	
***Cell Broadcast**	Yes	
Game	2 (Othello/Mobile hawk)	Or Black Jack
Calendar	Yes	Menu+6+1
Memo	20	Menu+6+2
World Clock	Yes	Menu+7+5
Unit Convert	Length/Surface/Volume/Weight	Menu+7+4
Fax & Data	Yes	
SIM Lock		Operator Dependent
SIM Toolkit	Class 1,2,3	

2.6 Test Standards

2.6.1 General Test

Category	Test Standard
Battery Sticking	10,000 times
Key Pad Printing	Load 1Kg Alcohol test 100 times
Salt Water Spray	Salinity 5%, (pH6.5~7.2) 35℃, 48Hr
Dust	Dust Size 75u Mech, Time : 1Hr
I/O Connector Sticking	3,000 times
Generation of Heat	In using - Near Ear & Cheek : below T=15℃ - Other parts : below T=25℃ In Charging – Near BATTERY : T=25℃
Voltage Change	±15%
Handle Strap Strength	12Kg
ESD Test	Air : 10㎸ (10 times per each parts)
Charging Contact Point Sticking	20 times/min
Key Press	300,000 times
Folder Open	50,000 times (20 times/min)

2.6.2 Drop Test

Packaged		Each face	Bottom face
	~10㎏	65㎝	75㎝
	10~20㎏	55㎝	70㎝
Non Packaged	150㎝ Wood plate, 3 times per each 6 faces		

2.6.3 Vibration Test

Packaged	1.5G (Amplitude3㎜) SWEEP RANGE 10~200㎐ SWEEP RATE : 0.25 Octave/min X, Y, Z 1 hour per each Axis
Non Packaged	1.5G (Amplitude3㎜) SWEEP RANGE 10~200㎐ SWEEP RATE : 0.25 Octave/min X, Y, Z 1 hour per each Axis

2.6.4 Environmental Test

Low Temperature Operation	-10℃ Humidity 0%, 12 Hr
High Temperature, High Humidity Operation	High Temperature & High Humidity Operation: 60℃ Humidity 85%,12Hr
Low Temperature Deposit	-30℃ Humidity 0%, 12 Hr
High Temperature, High Humidity Deposit	80℃ 80% 32Hr
Temperature, Humidity Cycle	25℃ 65% →50℃ 95% 24Hr 25℃ 65% 2Hr → -20℃ 24Hr: 1 cycle 25℃ 65% → 50℃ 95% 8Hr → -20℃ 8Hr → 25℃ 65% 2Hr: 3 cycles

3. TECHNICAL BRIEF

3.1 Digital Baseband (DBB) Processor

CALYPSO is a chip implementing the digital base-band processes of a GSM/GPRS mobile phone. This chip combines a DSP sub-chip (LEAD2 CPU) with its program and data memories, a Micro-Controller core with emulation facilities (ARM7TDMIE), internal 8Kb of Boot ROM memory, 4M bit SRAM memory, a clock squarer cell, several compiled single-port or 2-ports RAM and CMOS gates.
The application of this circuit is the management of the GSM/GPRS base-band processes through the GSM layer 1, 2 and 3 protocols as described in the ETSI standard with a specific attention to the power consumption in both GSM dedicated and idle modes, and GPRS (class 12) capability. The chip will fully support the GSM full-level test approval (FTA) for both Full-Rate, Enhanced Full-Rate and Half-Rate speech coding. CALYPSO implements all features for the structural test of the logic (full-SCAN, BIST, PMT, JTAG boundary-SCAN).

3.1.1 Block Diagram

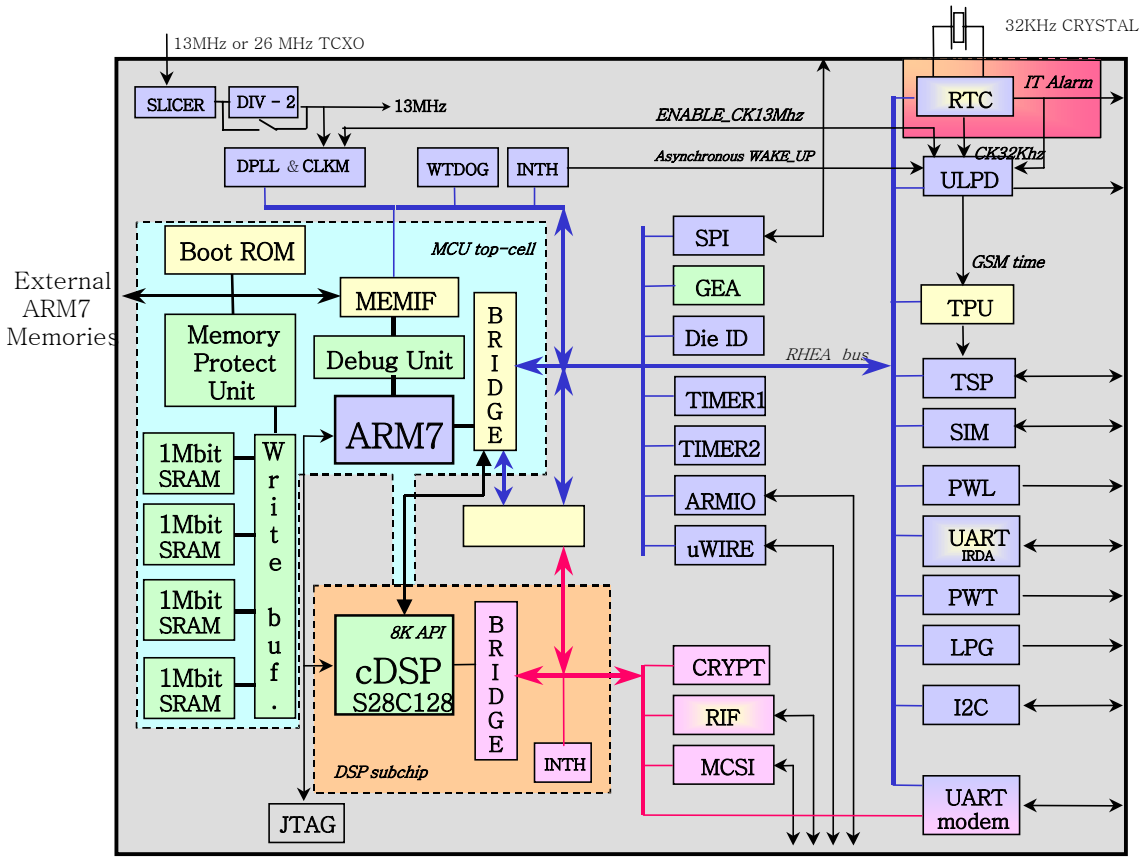


Figure 3-1-1. Block diagram of the Calypso G2(HERCROM400G2).

3.1.2 Block specification

CALYPSO architecture is based on two processor cores ARM7 and LEAD2 using the generic TI RHEA bus standard as interface with their associated application peripherals.
CALYPSO is composed from the following blocks:

- **ARM7TDMIE**
  ARM7TDMI CPU core (32/16 bits RISC processor)
  + ARM ice crusher for emulation purpose
- **DSP subchip S28C128**
  LEAD2 DSP core with 28K words of RAM and 128K words of ROM
  + API (8 Kw part of the 28K of RAM)
  + SPI
  + TIMER
- **Clock Squarer analog cell**.
- **ARM peripherals**:
  General purpose peripherals

• ARM Memory Interface for external RAM, Flash or ROM
• RHEA bridge
• 4 Mbit Static RAM with write-buffer
• Memory Protection Unit (MPU)
• Debug Unit (DU)
• 64 Kbit of via2-ROM for internal boot
• Die-ID cell (48 bits + 5 spare)

Application peripherals

• ARM General purposes I/O with keyboard interface and two PWM modulation signals for light and buzzer with possible tones generation.
• Micro Wire interfaces for LCD and EEPROM.
• 3 Timers (generic, watchdog)
• UART 16C750 interface (UART_IRDA) with
-. IRDA control capabilities (SIR)
-. Software flow control (UART mode).
-. hardware flow protocol (DCD, CTS/RTS)
• UART 16C750 interface (UART_MODEM) with
-. hardware flow protocol (DCD, CTS/RTS)
-. autobaud function
• SIM Interface
• ARM interrupts Handler (INTH).
• GSM real-time sequencer (TPU).
• GSM real-time Serial Port (TSP).
• DMA controller (4 channels – 2 ports)
• Real Time Clock (RTC)
• GSM Ultra Low-Power Device (ULPD)
• Clock generator & control with Digital Phase Locked Loop (CLKM)
• Programmable controller for Led pulse generation (LPG)
• Enhanced tone generator (PWT)
• Pseudo-noise modulator for light level control (PWL)
• Master I2C serial interface
• GPRS Encryption Algorithm module 1 & 2.

❑ ASIC DSP peripheral:

General purpose peripherals

• RHEA bridge

Application peripherals

• Radio interface (RIF).
• Multi Channels Serial Interface (MCSI)
• A51/A52 ciphering (CRYPT)
• UART 16C750 interface (UART_MODEM) with
-. hardware flow protocol (DCD, CTS/RTS)
-. autobaud function, local echo
• DMA controller (4 channels)
• DSP interrupts Handler (INTH).
❑ OTHER ASIC peripherals
• JTAG TAP controller.

3.1.2.1 ARM megacell (ARM7TDMIE)

The ARM7TDMI is a 32 bits RISC micro-controller core. This microprocessor works in 32 bits or 16 bit instructions and on 32, 16 or 8 bit data. The ARM7 architecture is based on reduced instruction set computer (RISC). Pipelining is employed so that all parts of the processing and memory systems can operate continuously. Typically, while one instruction is being executed, its successor is being decoded, and a third instruction is being fetched from memory. In CALYPSO chips family, ARM7 is intended to work in **'little endian'** mode only.

3.1.2.2 DSP sub chip(S28C128)

The DSP subchip is a Digital Signal Processor core compliant with the TMS320C54x family. The CPU core LEAD2 is associated with

- -. ARM Port Interface (API)
- -. An interrupt handler
- -. A parallel interface XIO
- -. A Timer
- -. 28K words of RAM including 8K words of API shared memory
- -. 128K words of ROM
- -. A serial port
- -. A JTAG interface

The input clock frequency is delivered by an external DPLL and the functional cycle frequency is planned to be in the range [0 – 91 MHz]

3.1.2.3 Clock squarer cell

The Clock Squarer cell is an analog cell which function is to reshape a clock signal provided by an external oscillator. The input signal is assumed to be a pseudo-sinusoidal signal with a limited dynamic transformed by the Clock Squarer cell in a square waveform with an amplitude of VCC.

3.1.3 Memory Interface

• 64Mbit x 2 Flash / 32Mbit Pseudo SRAM MCP
• 16 bit parallel data bus
• ADD01 ~ ADD22

Memory Interface : External/Internal Memory Interface
_CS0 : FLASH2, TH50VPF5783AASB,16bit access, 3 wait state
_CS1 : FLAHS1 in TH50VPF5783AASB, 16bit access, 3 wait state
_CS2 : Ext PSRAM, 16bit access, 3 wait state
_CS3 : Main LCD, Sub LCD, MIDI IC addressing, 16 & 8 bit access, 3 wait state
_CS6 : Int SRAM, 32bit access, 0 wait state

* Notes: *Calypso internal 39MHz machine 3wait state is necessary for the 80ns access because of 25ns machine cycle. (25*4 = 100ns)*

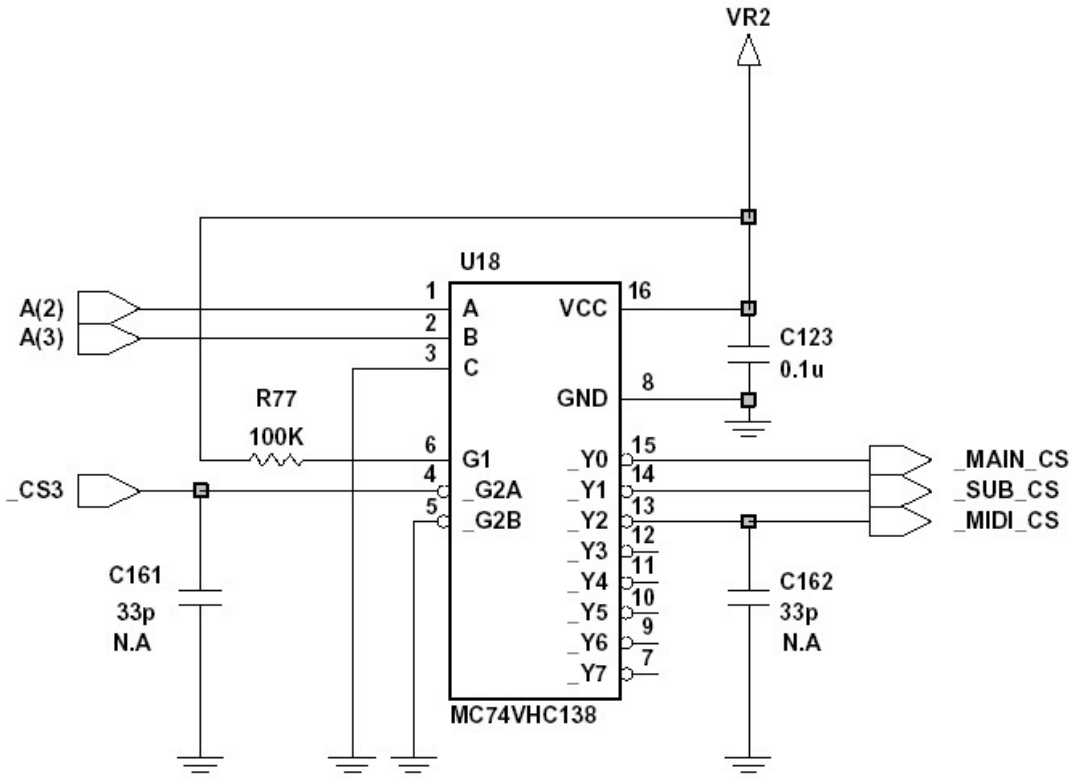


Figure 3-1-2. Decoding Circuit Diagram

3.1.4 External device connection

Table 3-1-1. External Device Interface

Interface					
Devices		Maker	Part No.	Write cycle time	Read cycle time
Memory	Flash 1	Toshiba	TH50VPF5783A ASB	70ns	70ns
	Flash 2			70ns	70ns
	PSRAM			70ns	70ns
Main LCD		SDI	UG12R61A		
Sub LCD		Samsung NEC			
MIDI		Yamaha	YMU762B	50ns	80ns

3.1.5 RF Interface

Table 3-1-2. RF Interface Specification

TSP (Time Serial Port)		
Resource	connection	Descriprion
TSPDO	ABB & Aero	Control data
TSPCLKX	Aero	Serial clock
TSPEN0	ABB & Aero	Data communication Enable
TSPEN1	Aero	Data communication Enable
TPU (Time Processing Unit) Parallel Port		
TSPACT0	Aero	Power down control signal
TSPACT1	Aero	PA on control signal
TSPACT2	Aero	Band selection control signal
TSPACT3	Antenna switch driver	Tx/Rx control signal
TSPACT4	Antenna switch driver	TxRx control signal

3.I.6 UART Interface

G7030 has two UART Drivers as follow :
UART1: Hardware Flow Control / Fax & Data Modem
UART2: Hands free Control / SW trace or IrDA Modem

Table 3-1-3. UART Interface Specification

UART1		
Resource	Name	Note
TX_MODEM	TXD	Transmit Data
RX_MODEM	RXD	Receive Data
CTS_MODEM	CTS	Clear To Send
RTS_MODEM	RTS	Request To Send
GPIO 3	DSR	Data Set Ready
GPIO 2	DCD	Data Carrier Detect
UART2		
TX_IRDA	TX	Transmit Data(UART2)
RX_IRDA	RX	Receive Data(UART2)
TXIR_IRDA	TXIR_IRDA	Infra-Red Transmit Pulse
RXIR_IRDA	RXIR_IRDA	Infra-Red Receive Pulse
SD_IRDA	SD_IRDA	IRDA transceiver Shut Down Mode

3.1.7 GPIO map

In total 16 allowable resources, G7030 is using 13 resources except 3 resources dedicated to SIM and Memory. G7030 GPIO(General Purpose Input/Output) Map, describing application, I/O state, and enable level, is shown in below table.

Table 3-1-4. GPIO Table

No. of I/O	Application	I/O	Resource state	Inactive state	Active state
I/O(0)	FOLDER	I	GPIO	High(Open)	Low(Close)
I/O(1)	MELODY_INT	I	GPIO	High	Low
I/O(2)	DCD	O	GPIO	Low	High
I/O(3)	DSR	I	GPIO	High	Low
I/O(4)	SUB_EN	O	GPIO	Low	High
I/O(5)	SIM_PWCTL	O	SIM		
I/O(6)	JACK_DETECT	I	GPIO	High	Low
I/O(7)	LCD_RESET	O	GPIO	High	Low
I/O(8)	SPK_EN	O	GPIO	Low	High
I/O(9)	MELODY_RESET	O	GPIO	High	Low
I/O(10)	LCD_DIM_CNTL	O	GPIO	High	Low
I/O(11)	KEYLIGHT	O	GPIO	Low	High
I/O(12)	TP27	I/O	GPIO		
I/O(13)	HANDSFREE	I	GPIO	High	Low
I/O(14)	_BHE	O	MEMORY		
I/O(15)	_BLE	O	MEMORY		

3.2 Analog Baseband (ABB) Processor

The TWL3012B device, along with a digital baseband (DBB) device, is intended for digital cellular telephone applications. This includes the GSM 900, the DCS 1800, and the PCS 1900 standards (dual-band capability).The TWL3012B device includes a complete set of baseband functions that perform the interface and processing of the following voice signals, the baseband in-phase (I) and the quadrature (Q) signals, which support both the single-slot and multi-slot modes. The TWL3012B device also includes associated auxiliary RF control features, supply voltage regulation, battery charging controls, and switch on/off system analysis. The TWL3012B device interfaces with the DBB device through a digital baseband serial port (BSP) and a voice-band serial port (VSP). The signal ports communicate with a DSP core (LEAD). A microcontroller serial port (USP) communicates with the microcontroller core and a time serial port (TSP) communicates with the time processing unit (TPU) for real-time control.
A specific module is dedicated to support the 3-V/5-V SIM card interface. This module includes the generation of the SIM card supply voltage as well as level shifters to adapt the SIM card signal levels to the microcontroller I/O signal levels. The TWL3012B device meets JTAG testability standard (IEEE Std 1131.1-1990) through a standard test access port (TAP) and boundary scan. The TWL3012B device also includes an on-chip voltage reference, under-voltage detection, and power-on reset circuits.

3.2.1 Block Diagram

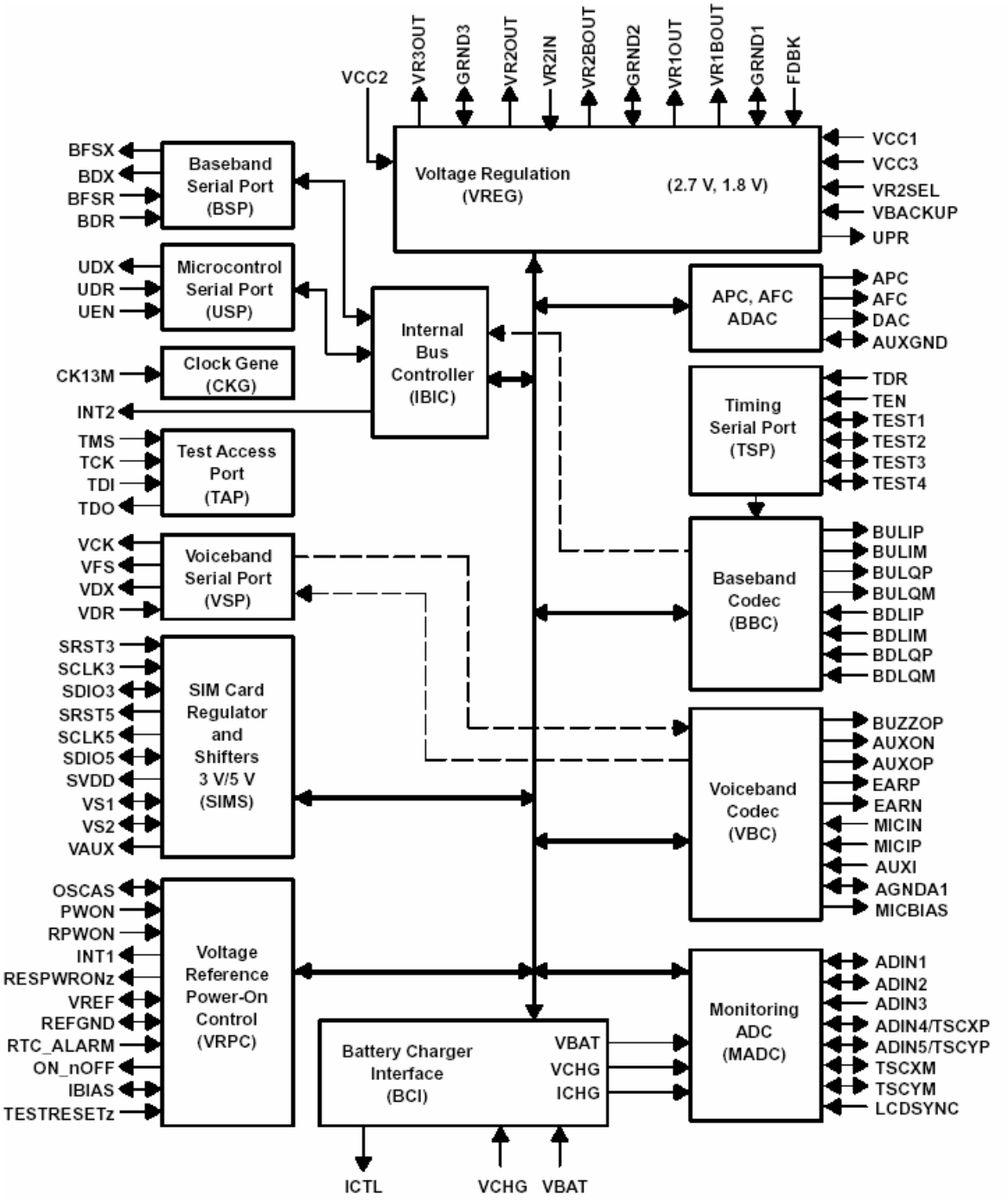


Figure 3-2-1. Block diagram of the Nausica

3.2.2 Features

The TWL3012B device supports the following features.
- Applications include GSM 900, PCS 1900, and DSC 1800 cellular telephones
- Voice coder/decoder (codec)
- Baseband codec single and multi-slot with I/Q RF interface
- Auxiliary RF converters
- SIM card interface
- Li-Ion or Ni-MH battery charging control
- Six low-dropout, low-noise, linear voltage regulators
- Voltage detectors (with power-off delay)
- Five-channel analog-to-digital converter (ADC)
- Low quiescent current

3.2.2.1 Voice Codec

The voice codec circuitry processes analog audio components in the voice uplink (VUL) path and applies this signal to the voice signal interface for eventual baseband modulation. In the voice downlink (VDL) path, the codec circuitry changes voice component data received from the voice band serial interface (VSP) into analog audio. The following paragraphs describe these uplink/downlink functions in more detail.

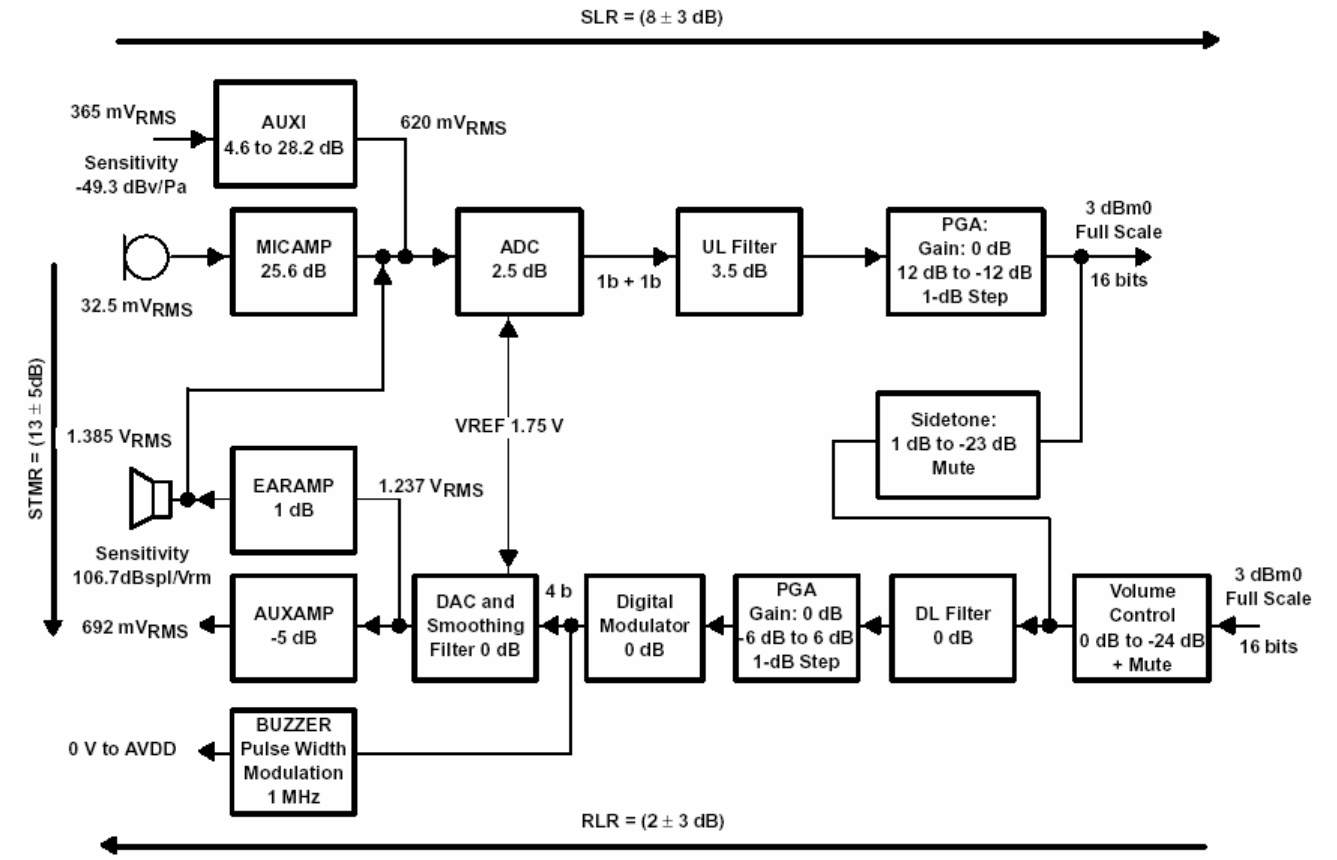


Figure 3-2-2. Voice Codec Block Diagram

3.2.2.1.1 Voice Uplink Path

The VUL path includes two input stages. The first stage is a microphone amplifier, compatible with electric microphones containing a FET buffer with open drain output. The microphone amplifier has a gain of typically 25.6 dB(±1 dB) and provides an external voltage of 2.0 V to 2.5 V to bias the microphone (K9, MICBIAS). The auxiliary audio input can be used as an alternative source for higher level speech signals. This stage performs single-ended-to differential conversion and provides a programmable gain of 4.6 dB to 28.2 dB. When auxiliary audio input is used, the microphone input is disabled and powered down.
The resulting fully differential signal is fed to the analog-to-digital converter (ADC) which is determined by the value of the internal voltage reference.
Analog-to-digital conversion is performed by a third-order Σ-.modulator with a sampling rate of 1 MHz. Output of the ADC is fed to a speech digital filter, which performs the decimation down to 8 kHz and band-limits the signal with both low-pass and high-pass transfer functions. Programmable gain can be set digitally from –12 dB to +12 dB in 1-dB steps and is programmed with bits 4–0 (VULPG(4:0)) of the voice-band uplink register (see Section 5.3.12.2). The speech samples are then transmitted to the DSP via the VSP at a rate of 8 kHz. There are 15 meaningful output bits.
Programmable functions of the VUL path, power-up, input selection, and gain are controlled by the BSP or the USP via the serial interfaces. The VUL path can be powered down by bit 0 (VULON) of the power down register.

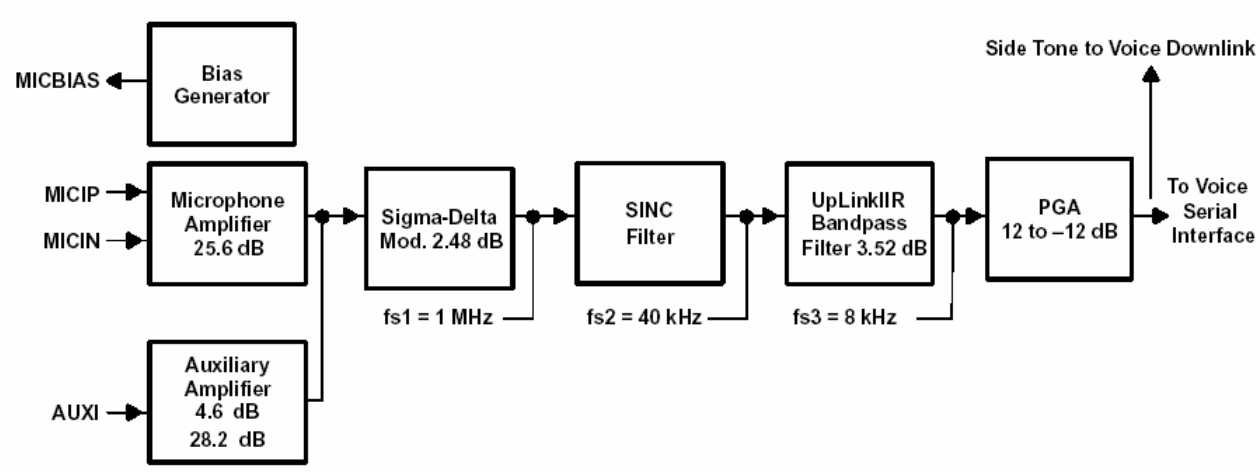


Figure 3-2-3. Voice Uplink Path

3.2.2.1.2 Voice Downlink Path

The VDL path receives speech samples at the rate of 8 kHz from the DSP via the VSP and converts them to analog signals to drive the external speech transducer.
The digital speech coming from the DSP is first fed to a speech digital filter that has two functions. The first function is to interpolate the input signal and to increase the sampling rate from 8 kHz up to 40 kHz to allow the digital-to-analog conversion to be performed by an over sampling digital modulator. The second function is to band-limit the speech signal with both low-pass and high-pass transfer functions. The filter can be bypassed by programming bit 9 (VFBYP) in the voice-band control register.
The interpolated and band-limited signal is fed to a second-order Σ-.digital modulator sampled at 1 MHz to generate a 4-bit (9 levels) over sampled signal. This signal is then passed through a dynamic element matching block and then to a 4-bit digital-to-analog converter (DAC).
Due to the over sampling conversion, the analog signal obtained at the output of the 4-bit DAC is mixed with a high frequency noise. Because a 4-bit digital output is used, a first-order RC filter (included in the 4-bit DAC) is enough to filter this noise.
The volume control and the programmable gain are performed in the TX digital filter. Volume control is performed in steps of 6 dB from 0 dB to –24 dB. In mute state, attenuation is higher than 40 dB. A fine adjustment of gain is possible from –6 dB to +6 dB in 1-dB steps to calibrate the system depending on the earphone characteristics. This configuration is programmed with the voice-band downlink control register.
The earphone amplifier provides a full differential signal on the terminals H9 (EARP) and H8 (EARN), and an auxiliary output amplifier provides a differential signal on terminals J9 (AUXOP) and J10 (AUXON). The VDL path can be powered down by bit 1 (VDLON) of the power down register.
The buzzer is driven on the board by a bipolar transistor. The output BUZZOP (terminal K10) delivers a 1-MHz pulse-width modulated bit stream that commands the base of the bipolar transistor.

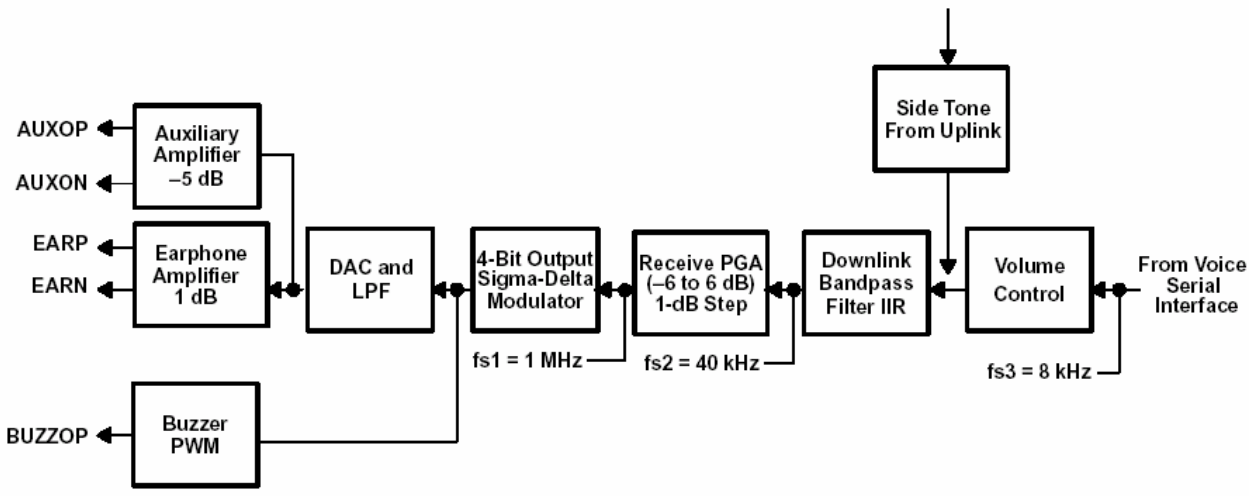


Figure 3-2-4. Voice Codec Downlink Path

3.2.2.1.2 Voice Downlink Path

The baseband codec includes a two-channel baseband uplink (BUL) path and a two-channel baseband downlink (BDL) path

3.2.2.2.1 Baseband Uplink Path

The modulator circuit in the BUL path performs the Gaussian minimum shift keying (GMSK) in accordance with the GSM specification 5.04. The data to be modulated flows from the DSP radio interface (RIF) through the baseband serial port (BSP).
The GMSK modulator is implemented digitally, the Gaussian filter computed on 4 bits of the input data stream being encoded in the sine/cosine look-up tables in ROM, and it generates the in-phase (I) and quadrature (Q) digital samples with an interpolation ratio of 16.
These digital I and Q words are sampled at 4.33 MHz and applied to the inputs of a pair of 10-bit DACs. The analog outputs are then passed through third-order Bessel filters to reduce out-of-band noise and image frequency and to obtain a modulated output spectrum consistent with GSM specification 05.05.
Fully differential signals are available at terminals C9 (BULIP), C10 (BULIM), D8 (BULQP), and D9 (BULQM).
To minimize phase trajectory error, the dc offset of the I and Q channels can be minimized using offset calibration capability. During offset calibration, input words of the 10-bit DACs are set to zero code and a 6-bit sub-DAC is used to minimize the dc offset at analog outputs.
The entire content of a burst, including guard bits, tail bits, and data bits, is stored in one of two 160-bit burst buffers before starting the transmission. The presence of two burst buffers is dictated by the need to support multi-slot transmission: one buffer is loaded with new data while the content of the second buffer is pushed into the GMSK modulator for transmission.
Single-slot or multi-slot mode is selected by bit 6 (MSLOT) of the baseband codec control register When single-slot mode is selected, only the content of burst buffer 1 is used for modulation.
Output level can be selected with bits 8 (OUTLEV1) and 7 (OUTLEV0) of the baseband codec control register.

The typical sequence of burst transmission consists of:
1. Power up the BUL path
2. Perform an offset calibration (not mandatory)
3. Modulate the content of the burst buffer

Timing of this sequence is controlled via the TSP, which receives a serial real-time control signal from the TPU of the digital baseband (DBB) device. Three real-time signals control the transmission of a burst: BULON, BULCAL, and BULENA. Each signal corresponds to a time window. BULON high sets the BUL path in power-on mode after a delay corresponding to the power-on settling time of the analog block. BULCAL enables the offset calibration window. During BULCAL, inputs of 10-bit DACs are forced to code zero and a low-offset comparator senses the dc level at terminals C9/C10 (BULIP/BULIM) and D8/D9 (BULQP/BULQM). The result of the comparison modifies the content of the offset registers, which drives the 6-bit sub-DACs to minimize the offset error. The duration of the calibration phase depends on the time needed to sweep the sub-DAC dynamic range. Modulation starts with the rising edge of BULENA and ends 32 one-quarter bits after the falling edge of BULENA. At the end of modulation, the modulator is reinitialized by setting the pointers of the burst buffers and the filter ROM to the base address. The I vector is set to its maximum value, while the Q vector is set to 0.
Power to unbalance the gain between I and Q channels allows compensation of natural gain mismatch or imperfection of RF mixer via bits 5 (IQSEL), 3 (G0), and 4 (G1) of the baseband codec control register. The output common mode voltage of terminals C9 (BULIP), C10 (BULIM), D8 (BULQP), and D9 (BULQM) can be set to VDD/2, to a fixed 1.35-V value, or to VGAP by bits 1 (SELVMID1) and 0 (SELVMID0) of the baseband codec control register.

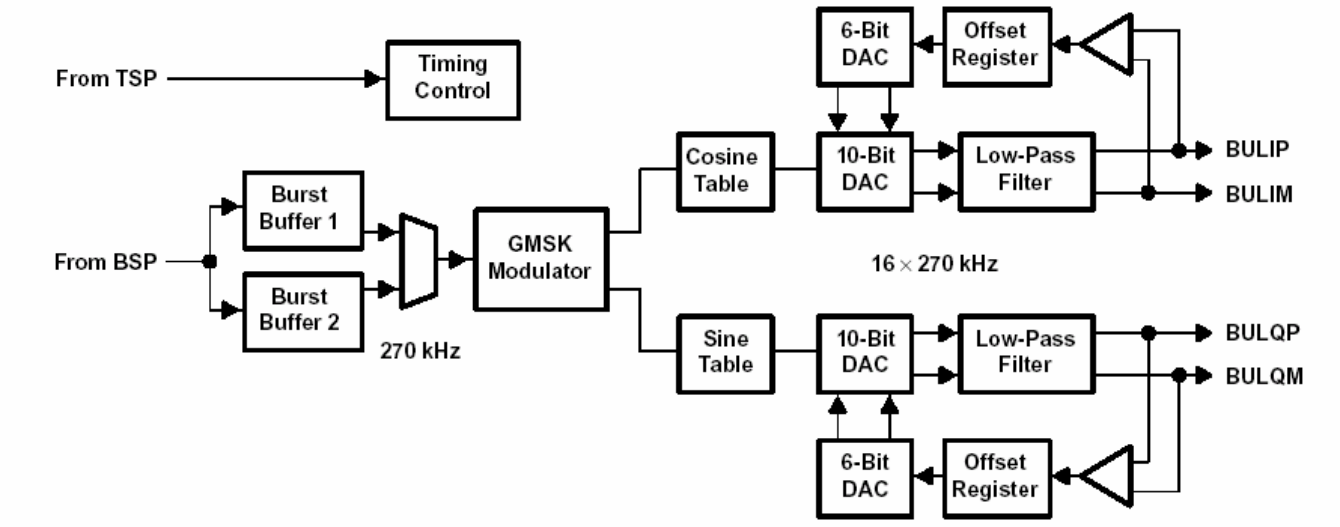


Figure 3-2-5. Baseband Uplink Block Diagram

3.2.2.2.2 Baseband Downlink Path

The baseband downlink (BDL) path includes two identical circuits for processing the analog baseband I and Q components generated by the RF circuits. The first stage of the BDL path is a continuous second-order anti-aliasing filter that prevents aliasing of out-of-band frequency components due to sampling in the ADC. This filter serves also as an adaptation stage between external and on-chip circuitry.

The anti-aliasing filter is followed by a third-order Σ-.modulator that performs analog-to-digital conversion at a sampling rate of 6.5 MHz. The ADC provides 2-bit words to a digital filter that performs the decimation by a ratio of 24 to lower the sampling rate to 270.8 kHz. The ADC also provides channel separation by providing enough rejection of the adjacent channels to allow the demodulation performances required by the GSM specification.

The BDL path includes an offset register, which stores the value representing the channel dc offset. This value is subtracted from the output of the digital filter before transmitting the digital samples to the DSP via the BSP. Upon reset, the offset register is loaded with 0s; its content is updated during the calibration process.

The typical sequence of burst reception consists of:
1. Power up the BDL path
2. Perform an offset calibration (not mandatory)
3. Convert and filter the I and Q components and transmit digital samples

Timing of this sequence is controlled via the TSP, which receives serial real-time control signals from the TPU of the DBB device. Three real-time signals control the transmission of a burst: BDLON, BDLCAL, and BDLENA. Each signal corresponds to a time window.

BDLON high sets the BDL path in power-on mode after a delay corresponding to the power-on settling time of the analog block. BDLCAL enables the offset calibration window. Two offset calibration modes are possible and are selected by the state of bit 9 (EXTCAL) of the baseband codec control register. When EXTCAL is 0, the analog inputs are disconnected from the external world and internally shorted. The result of conversion done in this state is stored in the offset register. When EXTCAL is 1, the analog input remains connected to external circuitry, and the result of conversion, including in this case internal offset plus external circuitry offset, is stored in the offset register. The duration of the calibration window depends mainly on the settling time of the digital filter.

Data conversion starts with the rising edge of the BDLENA signal; however, the first eight I and Q samples are not transmitted to the DSP, because they are not meaningful due to the group delay of the digital filter. The rising edge of BDLENA is also used by the IBIC to affect the transmit path of the BSP to the BUL path during the entire reception window. At the falling edge of BDLENA, the conversion in progress is completed and samples transmitted before stopping the conversion process. Finally, BDLON low sets the BDL path in power-down mode.

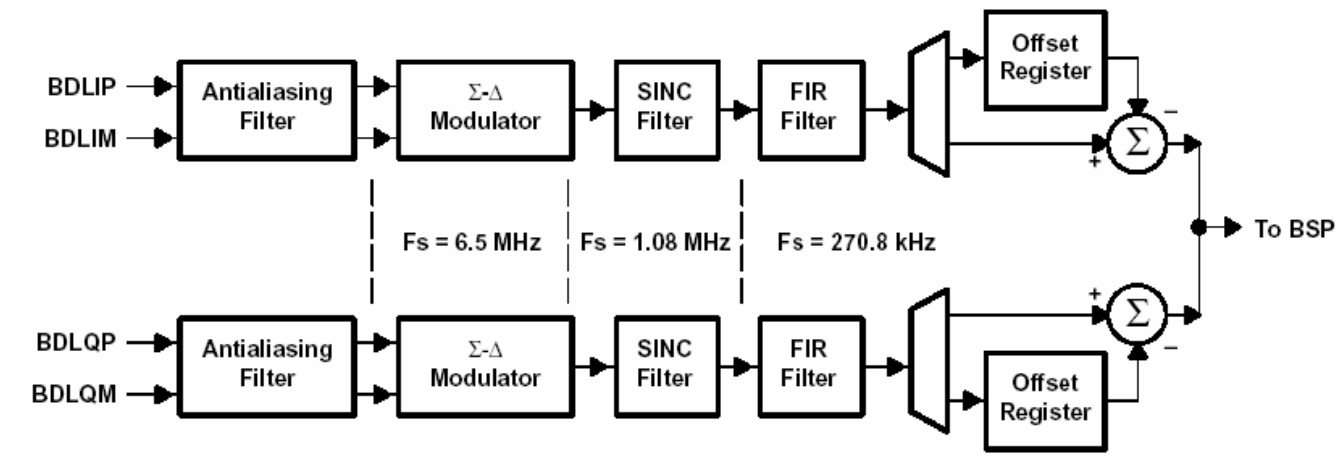


Figure 3-2-6. Baseband Downlink Block Diagram

3.2.2.3 TSP serial interface

The TSP serial interface allows the serial transmission of baseband control windows for the Nausica BBCODEC. It is managed through a TPU scenario hence it allows GSM quarter bit resolution and a precise positioning of CODEC commands among the GSM TDMA frame. Data format for this transmission is seven bits including UL/DL commands (On, Calibrate, Enable) and a start bit for ADC conversion. This command bit allows to place at precise moments in the TDMA frame the start of the ADC conversion.
Nausica register are not accessible through this serial link, sense of transmission is from Calypso to Nausica only. Aero (Si Lab) serial interface is also connected to Calypso TSP. Through this link the Calypso device programs synthesizers, the receiver, the offset PLL and the P.A. controller. TSP serial clock runs at 6.5MHz.

3.2.2.4 RIF/BSP serial interface

This interface is dedicated to the UL and DL transmission of I/Q samples between the DSP and the BBCODEC and to Nausica register access.On the UL path the DSP sends to the CODEC the burst bits to be modulated while on the DL path it receives non demodulated I/Q samples.

Write access to Nausica register is done using the same data format as the UL. Main functions executed are:
• APC parameters programmation (levels, delays, ramp coefficients)
• AFC
• Voice CODEC control

Register accesses could be considered synchronized to the TDMA frame as the DSP receives commands on TDMA frame start boundary. Clock frequency of RIF/BSP serial link is 13 MHz. BSP access are not allowed when ACTIVMCLK='0'.

3.2.2.5 ARM SPI/USP serial interface

This interface is dedicated to Nausica read and write register which accesses from Calypso. Through this link is possible to access all Nausica register, hence this port is used to configure and to manage the status of each block of Nausica device. Also ADC result of conversion can be read through this interface. This access is asynchronous to the TDMA frame and has a higher priority than the BSP access. Possible conflicts due to simultaneous access from ARM SPI and LEAD RIF are managed by the Nausica IBIC. This serial link runs at 13 MHz.

3.2.2.6 LEAD SPI/VSP serial interface

This interface allows voice samples exchanges in DL and UL direction between the DSP and the Nausica Voice Band CODEC. Nausica VSP is the master port in the transmission, serial link runs at 500kHz.

3.2.2.7 JATG Interface

The test access port (TAP) meets JTAG testability standard (IEEE Std1131.1-1990). TAP allows public instructions set of JTAG standard and also private instructions to configure the device in special modes for test or debug purpose.

3.2.2.8 Clocks

Nausica device receives two clocks from Calypso: A slow clock CLK32K_OUT used by the DBB as reference clock for low power modes(back-up, deep-sleep).
The ABB adopt this clock as the VRPC synchronous state machine clock and as reference clock when fast clock is not present. A fast clock CLK13M_OUT used by the DBB and ABB as reference clock for all modules including serial transmission.

The 32KHz Crystal is connected between input and output of the oscillator (OS32K_IN and OSC32K_out pins). Connection has been shortest as possible. The two load capacitors are connected on the crystal and common point (ground return current) has to be connected to the dedicated oscillator ground VSSO.

Filtering capacitor of the oscillator power supply must be connected to VSSO pin (same point as crystal load capacitor return point) and directly to the nearest VDDRTC pin using connection length as short as possible. This is to prevent frequency jitter performances to be affected by the power supply noise induced by fast internal logic transitions.

3.2.2.9 Interrupts

Nausica device is able to generate two kinds of interrupts:
• An emergency interrupt connected to Calypso EXT_FIQ signaling the detection of allow battery voltage.
• An event detection interrupt connected to Calypso EXT_IRQ signaling :
- . Falling or rising edge at RPWON pin.
- . Falling edge at PWON pin.
- . Termination of an analog to digital conversion.
- . Charger plug.

3.2.2.10 Power Managements

Those three signals controls system status and system status transitions, they are supplied on the VRRTC power domain.
• nRESPWONZ signal
-. Is generated by the ABB
-. Is the reset of the power split part of the DBB chip.
-. It is active only one time (as long any kind of supply, BB or MB is present) at the first start of the mobile. Split power logic will provide to propagate this signal as global reset as soon as power supply will be present on the rest of the chip.

• ON_nOFF signal
-. Is generated by the ABB
-. the ASIC modules, ARM, LMM, reset.
-. It is at logical low level each time the system is switched off. Also this signal is managed by the split power logic and propagated to the rest of the circuit.

• ITWAKEUP signal
-. Is generated by the DBB
-. Is used to wake up the system from low power modes (backup, deep sleep).
-. It is built as a combination of all the interrupt request that are allowed to awake the Calypso ULPD module and the RTC alarm.

3.2.2.11 Voltage Regulation(VREG)

There are 5 LDO(Low Drop Output) regulators in ABB chip. The output of these 5 LDOs are as following table. (Figure 3-6) shows the power supply related blocks of DBB/ABB and their interfaces in G7030.

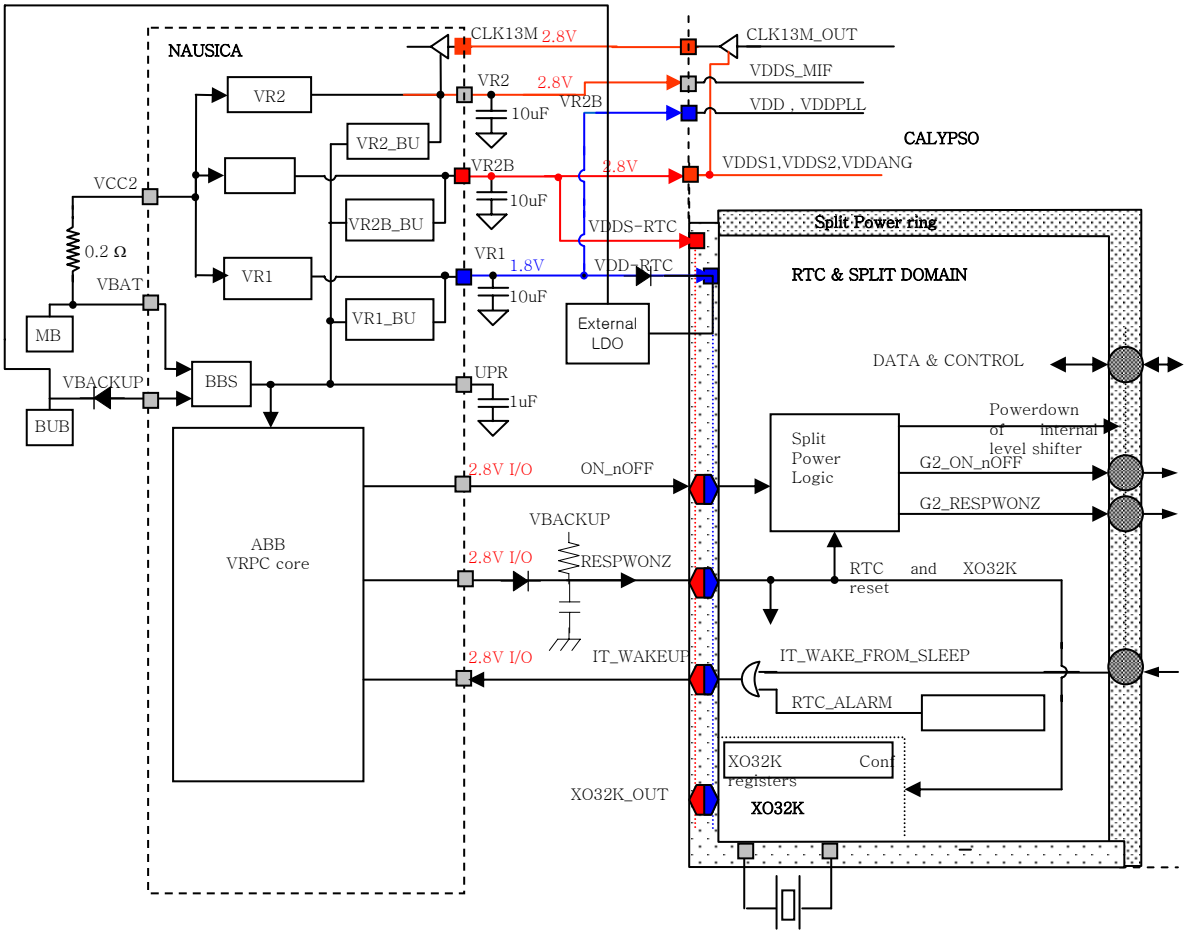


Figure 3-2-7 Compatibility connection with Nausica

Table 3-2-1. LDO Output Table

	Output Voltage	Usage
VR1	1.8V	Digital Core of DBB
VR1B	2.0V	Digital Core of ABB
VR2	2.85V	Memory Interface of DBB
VR2B	2.85V	Digital I/Os of DBB & ABB
VR3	2.85V	Analog Block of ABB

3.2.2.12 ADC Channels

ABB ADC block is composed of 4 internal ADC(Analog to Digital Converter) channels and 5 external ADC channel. This block operates charging process and other related process by reading battery voltage and other analog values.

Table 3-2-2. ADC Channel Spec

ADC 9 channels		
Resource	**Name**	**Note**
VCHG	VCHG	Charging management
VBAT	VBAT	
ICHG	ICHG	
VBACKUP	VBACKUP	Backup battery
ADCIN1	Not use	
ADCIN2	BATT_TEMP	Main battery temp. sensing
ADCIN3	RADIO_TEMP	RF temp. sensing
ADCIN4/TSCXP	HOOK_DETECT	Hook button sensing
ADCIN5/TSCYP	Not use	

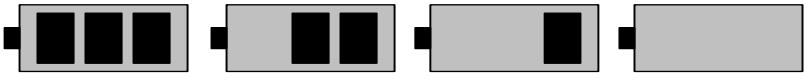
3.2.2.13 Power Supplies

The schematic above shows Nausica to Calypso power supply connections. Items to be highlighted on that schematic are the following:

- . MB is not connected no supply will be provided at the output of those LDO's.
- . The back up regulator RRTC is always enabled and provides supply to the Calypso "power split" domain on every functional mode of the system.
- . RRTC and RDBB can be selected between 1.4V and 1.8V through the VLRTC input pin.
- . Default voltage value of RMEM can be selected between 2.8V and 1.8V through the VLMEM input pin.
- . RDBB regulator allows external voltage sensing for sharper regulation on the VSDBB input pin. This allows elimination of the pad and wire connection drop to the Calypso power supply input. To make this feature effective, return sense point must be chosen as next as possible to Calypso input.
- . In Nausica to Calypso application RTC I/O's level shifters are used with same voltage value at both sides => VDD-RTC = VDDS-RTC = 1.8V.

3.2.2.14 Charging

Charging block in ABB processes charging operation by using VBAT, ICHG value through ADC channel. Battery Block Indication and SPEC of G7030 is as follow.



4.2V~3.81V **3.81V~3.73V** **3.73V~3.62V** **3.62V~3.35V**

Figure 3-2-7. Battery Level Indicator

1. Charging method: CC-CV
2. Charger detect voltage: 4.0V
3. Charging time: 2h
4. Icon stop current: 65mA
5. Charging current: 480mA
6. CV voltage: 4.2V
7. Cutoff current: 40mA
8. Full charge indication current (icon stop current) : 65mA
9. Recharge voltage: 4.16V
10. Low battery alarm
    a. Idle: 3.62V b. Dedicated: 3.50V
11. Low battery alarm interva :
    a. Idle: 3min b. Dedicated:1min
12. Switch-off voltage: 3.35V
13. Charging temperature ADC range
    a. Room temperature < -5centigrade: not charging operation.
    b. -5centigrade < Room temperature< 45centigrade: charging.
    c. 45centigrade< Room temperature: not charging operation.

3.2.2.15 SIM Interface

The SIM Card digital interface in ABB insures the translation of logic levels between DBB and SIM Card, for the transmission of 3 different signals:
-. A clock derived from a clock elaborated in DBB, to the SIM-Card (DBBSCK SIM_CK)
-. A reset signal from DBB to the SIM Card (DBBSRST SIM_RST).
-. A serial data from DBB to the SIM Card (DBBSIO SIM_IO) and vice-versa.

The SIM card interface can be programmed to drive a 3V or 5V SIM Card.

Table 3-2-3. SIM Interface

SIM (Interface between DBB and ABB	
SIM_RST	SIM card async/sync reset
SIM_PWCTRL	SIM card power activation
SIM_IO	SIM card bidirectional data line
SIM_CLK	SIM card reference clock

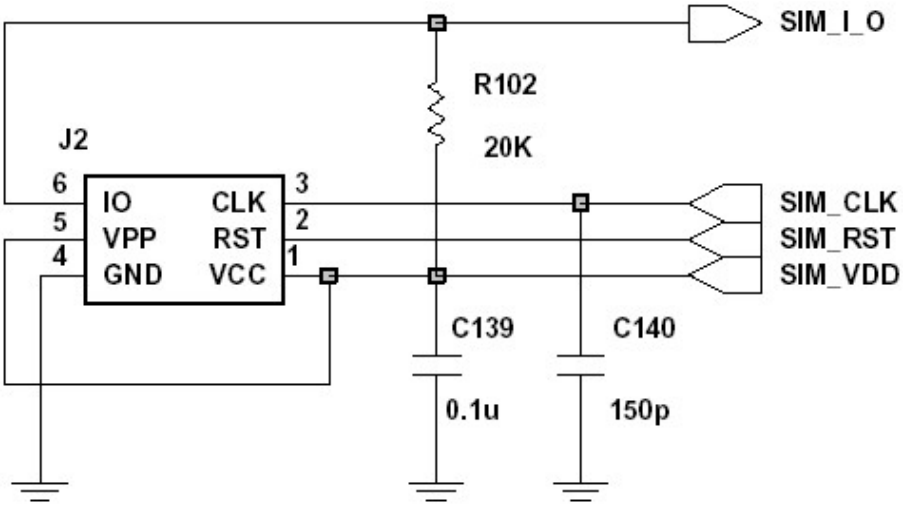


Figure 3-2-8. SIM Interface

3.3 Display & FPC Interface

LCD module is connected to main board via 34 pin Flexible PCB. It includes dual mode speaker, vibrator and backup battery.

Figure 3-2-8. SIM Interface

No	Pin Name	Category	Function
1	D15	Data bus	Data input
2	D14		Data input
3	D13		Data input
4	D12		Data input
5	D11		Data input
6	D10		Data input
7	D09		Data input
8	D08		Data input
9	VR2B	Power	Power Supply (Main & Sub)
10	MAIN_BACKLIGHT	Backlight	Main LCD Backlight
11	GND	Power	Ground
12	SUB_EN	Enable	Sub LCD EN
13	VBACKUP	Power	Backup Battery
14	MOTOR	Vibrator	Vibration Control
15	GND	Power	Ground
16	SPKN	Audio	Speaker & Receiver N
17	SPKP	Audio	Speaker & Receiver P
18	GND	Power	Ground
19	GND	Power	Ground
20	LCD_DIM_CNTL	Dimming	Main LCD Dimming Control Pin
21	LCD_RESET	Reset	Reset (Main & Sub)
22	_MAIN_CS	Chip select	Main LCD Chip select
23	_SUB_CS	Chip select	Sub LCD Chip select
24	VBAT	Power	Battery Voltage
25	_WR	Write	Main LCD Write Control
26	A(1)	Switch	Switch Data or Command
27	D07	Data bus	Data input
28	D06		Data input
29	D05		Data input
30	D04		Data input
31	D03		Data input
32	D02		Data input
33	D01		Data input
34	D00		Data input

3.4 Audio Interface

3.4.1 Microphone circuits

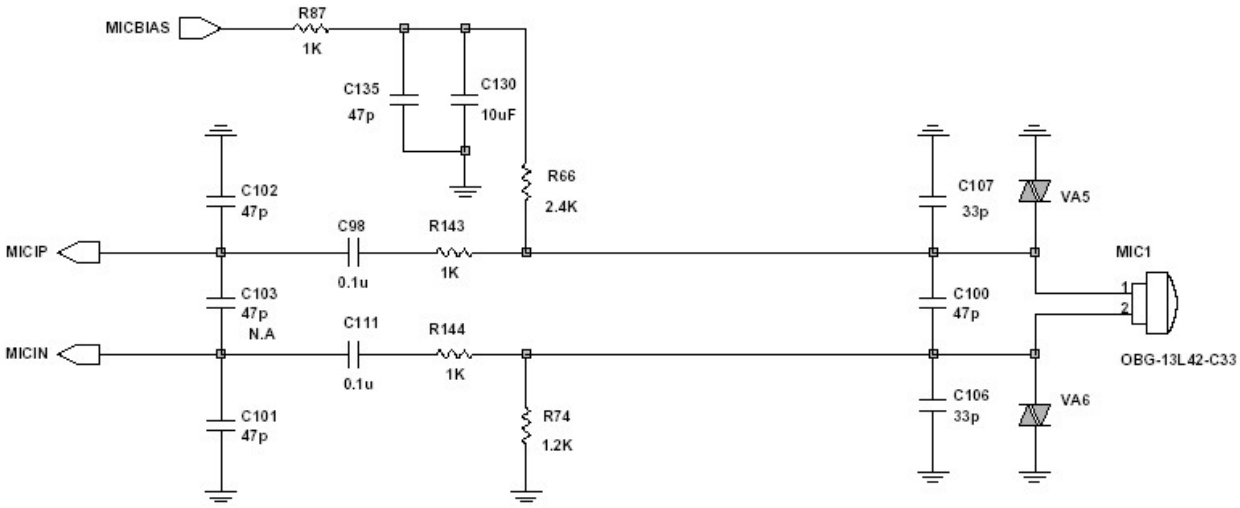


Figure 3-4-1. Microphone system

When a call is established, MICBIAS signal goes up to '2.0V' in the G7030. Nausica(ABB) provides both 2.0V and 2.5V for MICBIAS to circuit designer. VA5, VA6 are employed to enhance ESD immunity.

3.4.2 Head set Jack Interface

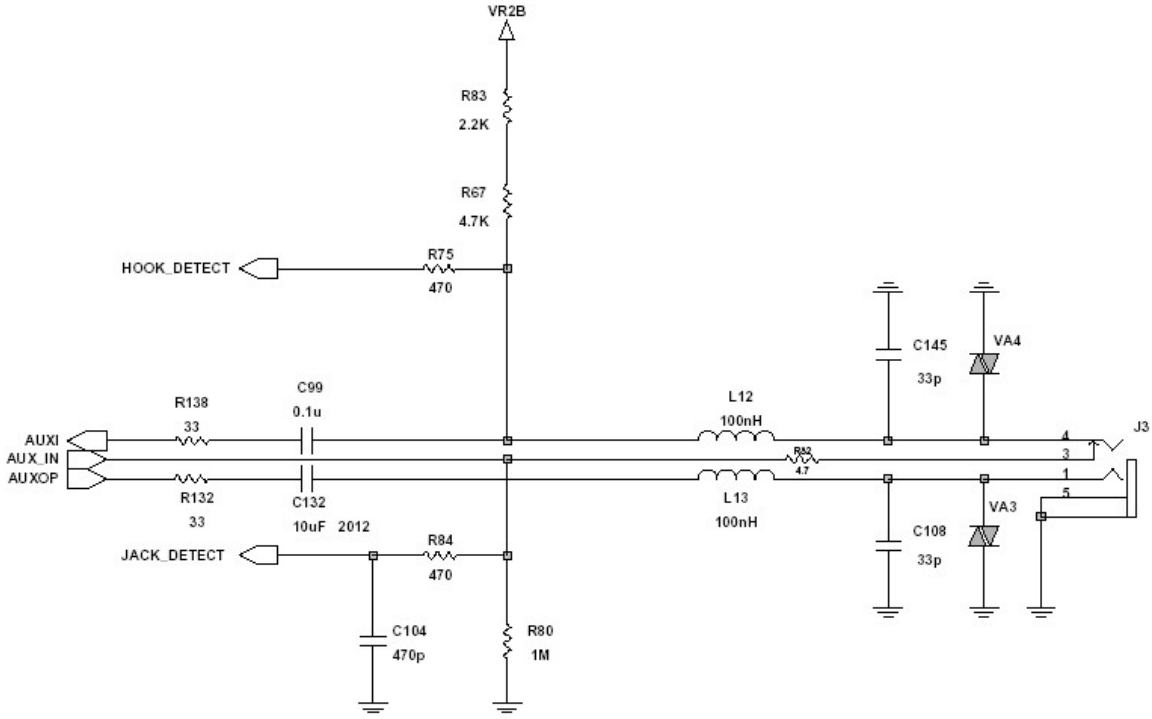


Figure 3-4-2. Ear-Jack interface

When ear-mic set or head set plug is inserted into the receptacle, JACK_DETECT signal change from ‘H’ to ‘L’. If hook button is pushed for a second to make a call, then HOOK_DETECT signal goes from ‘H’ to ‘L’. Also call end has same mechanism by pushing hook button on the Ear-microphone strap. Ordinarily detection of pushing hook button is established by signal de-bouncing for about 20ms.

3.4.3 Speaker Circuits

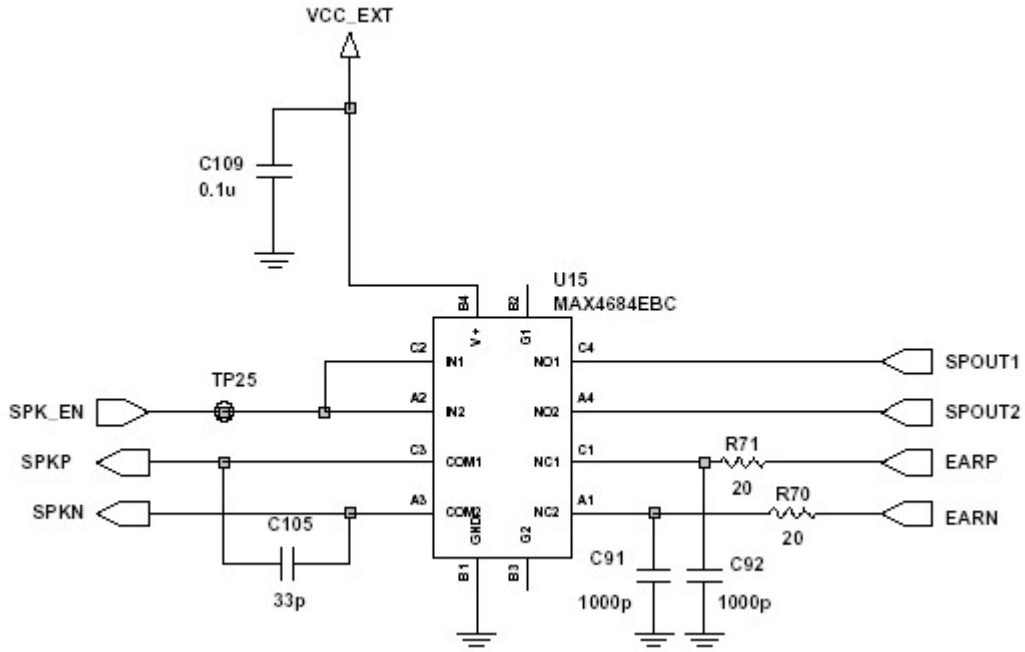


Figure 3-4-3. Dual mode speaker system switch

Single package dual analog switches are employed to support both voice and MIDI sound mode with one speaker. The speaker is designed to support both receiver and loud speaker characteristics. If the SPK_EN port sets ‘H’, then the speaker will operate as loud speaker. The other case, the SPK_EN port will remain ‘L’ state

3.4.4 MIDI SOUND circuit description

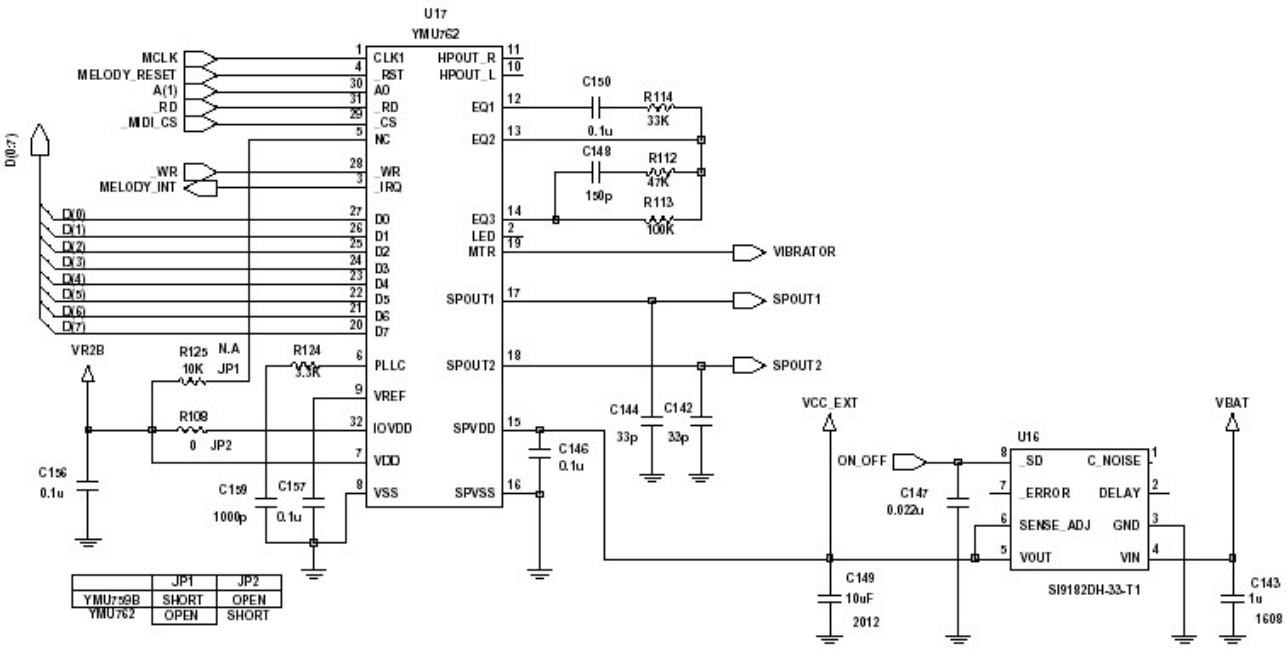


Figure 3-4-4. Dual mode speaker system switch

Midi synthesizer circuit includes YMU762B, external regulator(3.3V output) and jumpers to selection guide both YMU759B and YMU762B, R125, R108 are used alternatively. At present R108 is used to support YMU762B(40 poly MIDI sound).

3.4.4.1 The YMU762B has features as described below.

-. Simultaneous generation of up to 40 tones:
-. Polyphonic synthesizer specification
-. Has built-in default tones for FM and Waveform table synthesizers in the ROM, and the tones can be downloaded to RAM.
-. Stream replay with ADPCM/PCM
-. Software interrupt mechanism for external synchronization
-. Equipped with 8 bit parallel I/F for control from CPU
-. Equipped with speaker amplifier and equalizer circuit
-. Has built-in PLL to support inputting of master clock up to 20 MHz.
-. Contains a 16-bit stereophonic D/A converter.

3.5 Key Pad back-light Illumination

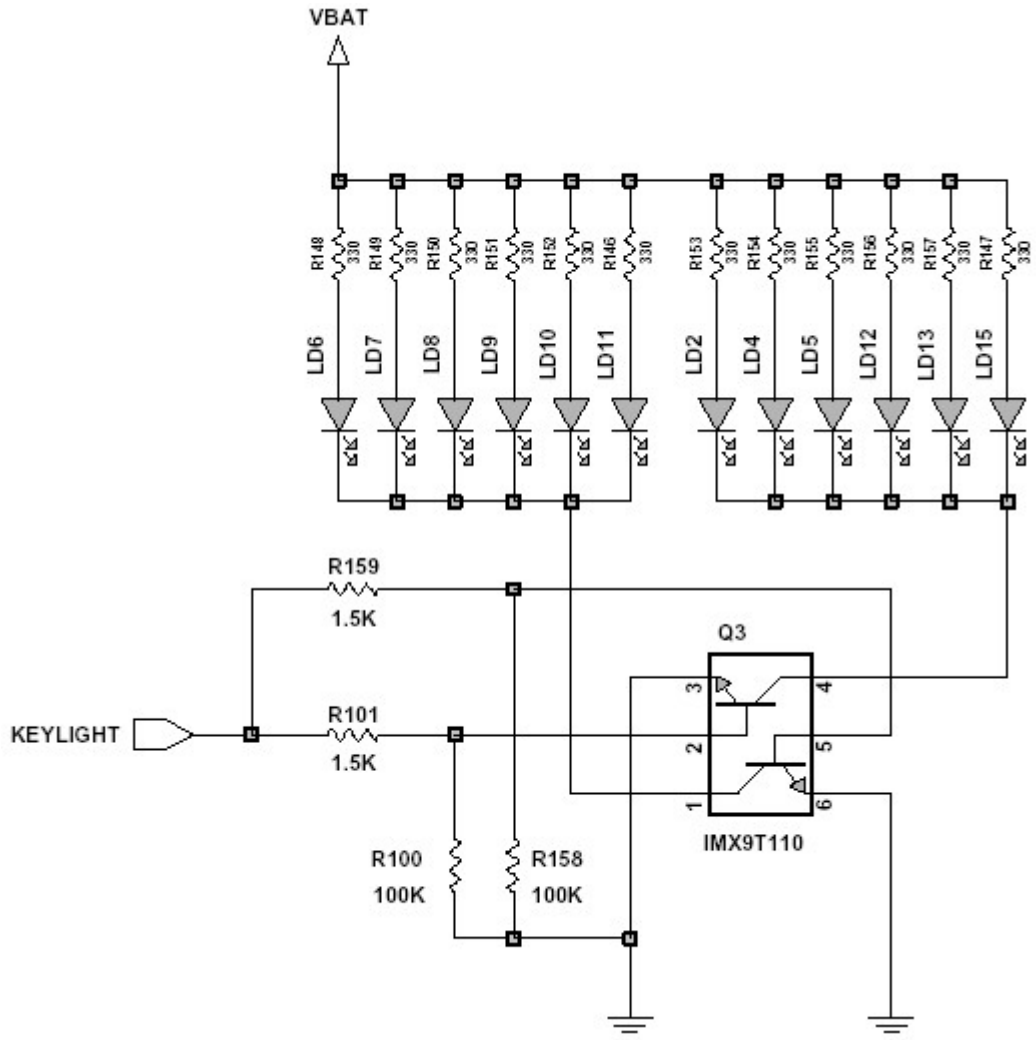


Figure 3-5-1. Key pad back light switch

KEYLIGHT signal controls Key backlight switching system. The user can change the time duration of back light 'ON'. When backlight is turned on , the current consumption is about 30mA(@ VBAT = 3.7V) from the main battery.

3.6 Keyboard connection

DBB supports 25 Key map and Switch-ON Key is directly connected to ABB(see Figure 6-1)

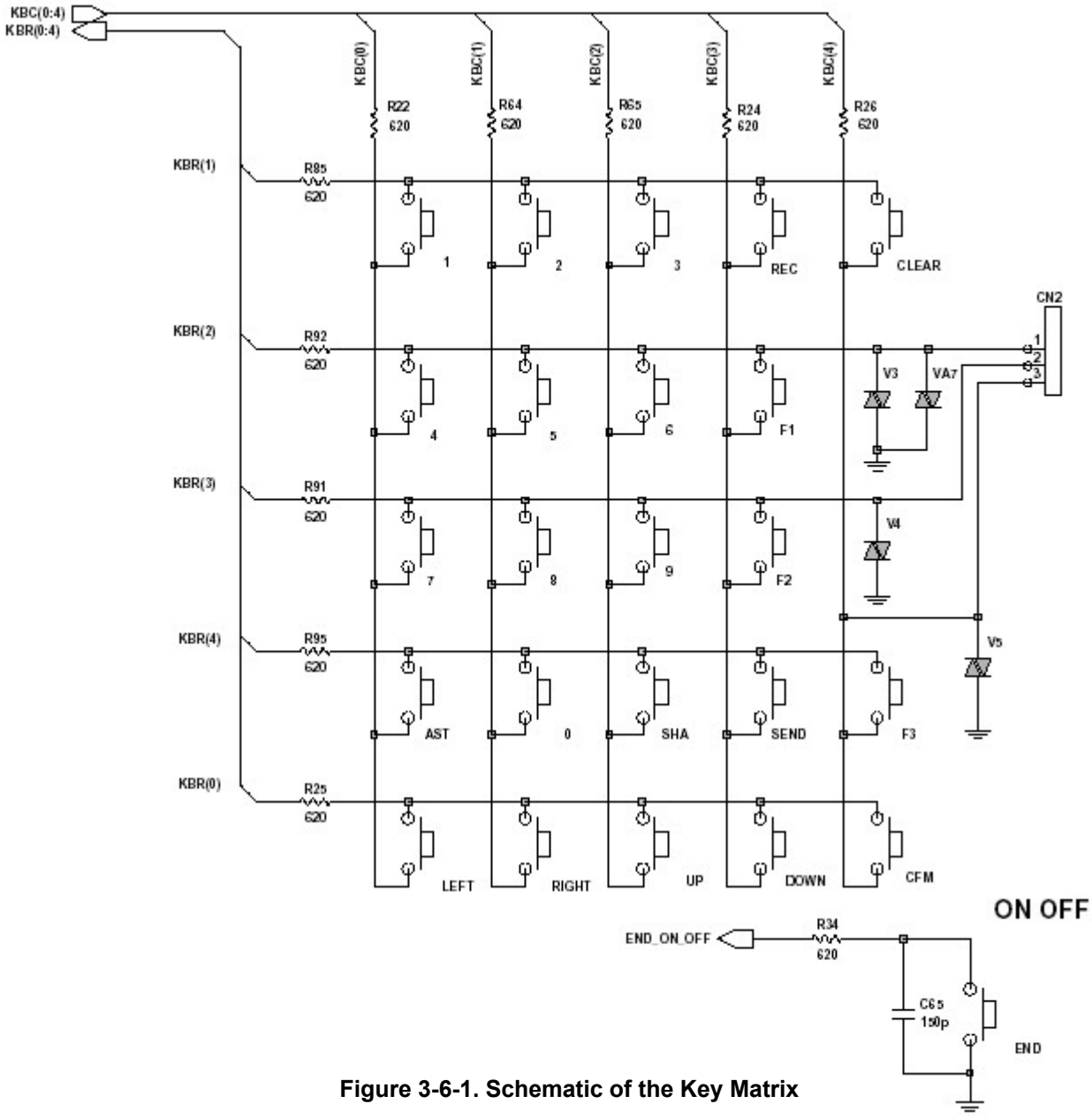


Figure 3-6-1. Schematic of the Key Matrix

The keyboard is connected to the chip using:
-. KBR (4:0) input pins for row lines
-. KBC (4:0) output pins for column lines

If a key button of the keyboard matrix is pressed, the corresponding row and column lines are shorted together to allow key press detection. All input pins (KBR) are pulled up to VCC internally and all of KBC are driving a low level. Any action on a button will generate an interrupt to the microcontroller which will, as answer, scan the column lines with the sequence.
In this scheme, G7030 supports 25 Key and Power key detection(ON_OFF) is executed by Nausica.

3.7 RF Transceiver part General Description

The RF parts consist of a transmitter part, a receiver part, a frequency synthesizer part, a voltage supply part, and a VCTCXO part. The Aero transceiver is composed of three RF chipsets,Si4200-BM[U6],Si4133T-BM[U5] and Si4201-BM[U7] which is a dual and triple-band GSM/GPRS wireless communications. This device integrated a receiver based on a low IF(100KHz) architecture and a transmitter based on a modulation loop architecture. And, the synthesizer[U5] part employed the Silicon Labs Si4133T-BM, a complete dual band synthesizer with built in VCOs. The transceiver employed a 3 wire serial interface to allow an external system controller to write the control registers for dividers, receive path gain, power down setting, and other controls.

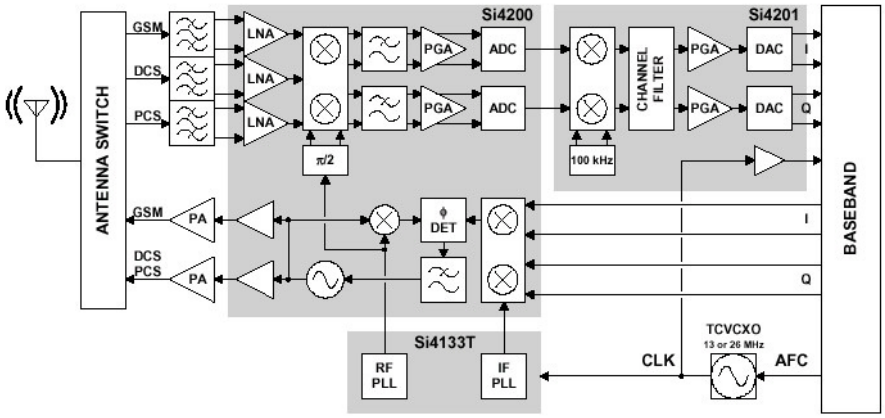


Figure 3-7-1. RF Front End Block Diagram

3.7.1 Receiver Part

The receiver part uses a low-IF receiver architecture that allows for the on-chip integration of the channel selection filters, eliminating the external RF image reject filters and the IF SAW filter required in conventional super-heterodyne architecture. The Si4200-BM[U6] integrates three differential input LNAs that are matched to the 200 Ohm balanced-output SAW filters through external LC matching networks. A quadrature image-rejection mixer downconverts the RF signal to a 100kHz intermediate frequency(IF) with the RFLO from the Si4133T-BM[U5]. The mixer output is amplified with an analog programmable gain amplifier(PGA) and quadrature IF signal is digitized with high resolution A/D converters(ADCs). The Si4201-BM[U7] downconverts the ADC output to baseband with a digital 100kHz quadrature LO signal. Digital decimation and IIR filters perform channel selection to remove blocking and reference interference signals. After channel selection, the digital output is scaled with digital PGA, which is controlled with the DGAIN[5:0] bits in register 05h.The amplified digital output signal go through with DACs that drive a differential analog signal onto the RXIP,RXIN,RXQP and RXQN pins to interface to standard analog ADC input baseband ICs.

	Antenna Bar Number	Power(dBm)
Antenna Display	5	≥ -85
	4	≥ -90
	3	≥ -95
	2	≥ -100
	1	≥ -105
	0	< -105

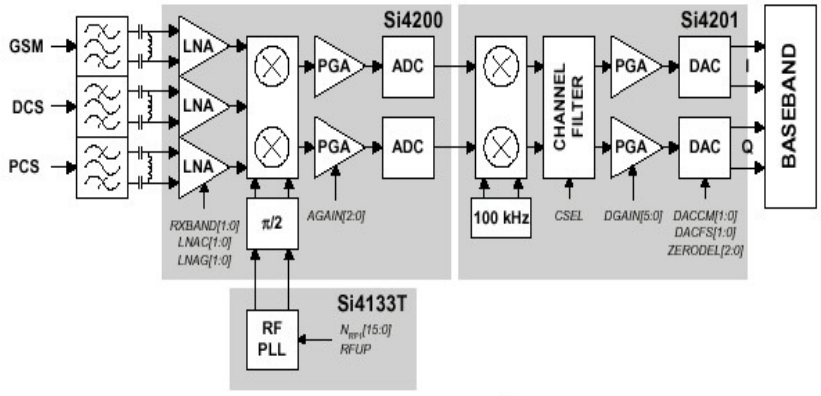


Figure 3-7-2. Receiver Block Diagram

3.7.2 Synthesizer Part

The synthesizer IC, the Si4133T-BM[U5] is a monolithic CMOS integrated circuit that performs IF and RF synthesis. Two complete PLLs are integrated including VCOs, varactors, resonators, loop filters, reference and VCO dividers, and phase detectors. Differential outputs for the IF and RF PLLs are provided for direct connection to the Si4200-BM[U6] transceiver IC. The RF PLL uses two multiplexed VCOs.

The RF1 VCO is used for Receive mode, and the RF2 VCO is used for Transmit mode. The IF PLL is used only during Transmit mode and uses a single VCO. The center frequency of each of the three VCOs on the Si4133T is set by connection of an external inductance(Lext).
A programmable divider at the XIN pin allows either a 13 or 26MHz from the external applied crystal oscillator. The RF PLL phase detector update rate can be programmed with the RFUP bit in register 31h to either 100kHz or 200kHz. The IF PLL always uses 200kHz. Receive mode should use 100kHz in DCS1800 and PCS1900 bands, and 200kHz in the GSM850 and E-GSM 900 bands.

Transmit modes should always use 200kHz. The IF and RF output frequencies are set by programming the N-Divider registers and also programmed via 3-wire interface with external system controller.

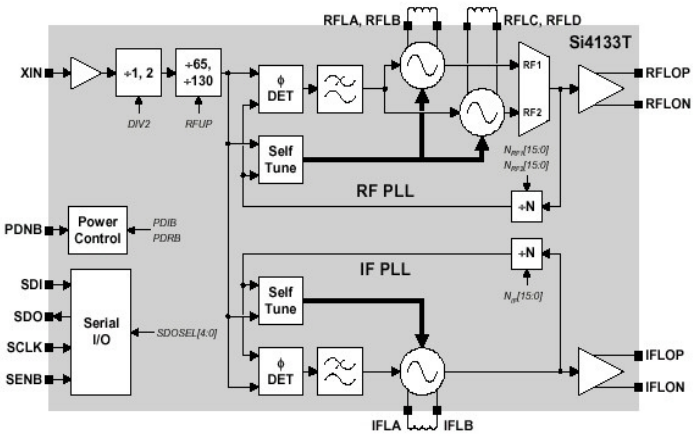


Figure 3-7-3. Si4133T Frequency Synthesizer Block Diagram

3.7.3 Transmitter Part

The transmit section of Si4200-BM [U6] consists of an I/Q baseband upconverter, an offset phase-locked loop (OPLL) and two 50 ohm output buffers that can drive external power amplifiers (PA). The OPLL requires no external duplexer to attenuate transmitter noise and spurious signals in the receive band. Additionally, the output of the transmit VCO (TXVCO) is a constant-envelope signal which reduces the problem of spectral spreading caused by nonlinearity in the PA. A quadrature mixer upconverts the differential I/Q signals with the IFLO to generate a SSB IF signal which is filtered and used as the reference input to the OPLL. The Si4133T [U5] generates the IFLO frequency. The IFLO is divided by two to generate the quadrature LO signals for the quadrature modulator. The OPLL consists of a feedback mixer, a phase detector, a loop filter, and a fully integrated TXVCO. The TXVCO is centered between the DCS 1800 and PCS 1900 bands, and its output is divided by two for the GSM 850 and E-GSM 900 bands. The Si4133T generates the RFLO frequency between 1272 and 1483 MHz. To allow a single VCO to be used for the RFLO, High-side injection is used for the GSM 850 and E-GSM 900 bands, and low-side injection is used for the DCS 1800 and PCS 1900 bands. Low-pass filters before the OPLL phase detector reduce the harmonic content of the quadrature modulator and feedback mixer outputs. The cutoff frequency of the filters is programmable with the FIF[3:0] bits in register 04h.

The RF3133 [U4] is a triple-band GSM/DCS/PCS power amplifier module that incorporates an indirect closed loop method of power control. The indirect closed loop is fully self contained and does not require loop optimization. It can be driven directly from the DAC output in the baseband circuit. On-board power control provides over 35 dB of control range with an analog voltage input; and, power down with a logic "low" for standby operation. It's efficiency is 55% at GSM and DCS.

GSM 900 transmitter output power

Power control level	Transmitter output power	Tolerances	
	dBm	normal	extreme
5	33	±3 dB	±4 dB
6	31	±3 dB	±4 dB
7	29	±3 dB	±4 dB
8	27	±3 dB	±4 dB
9	25	±3 dB	±4 dB
10	23	±3 dB	±4 dB
11	21	±3 dB	±4 dB
12	19	±3 dB	±4 dB
13	17	±3 dB	±4 dB
14	15	±3 dB	±4 dB
15	13	±3 dB	±4 dB
16	11	±5 dB	±6 dB
17	9	±5 dB	±6 dB
18	7	±5 dB	±6 dB
19	5	±5 dB	±6 dB

GSM 900 transmitter output power

Power control level	Transmitter output power	Tolerances	
0	30	±3 dB	±4 dB
1	28	±3 dB	±4 dB
2	26	±3 dB	±4 dB
3	24	±3 dB	±4 dB
4	22	±3 dB	±4 dB
5	20	±3 dB	±4 dB
6	18	±3 dB	±4 dB
7	16	±3 dB	±4 dB
8	14	±3 dB	±4 dB
9	12	±4 dB	±5 dB
10	10	±4 dB	±5 dB
11	8	±4 dB	±5 dB
12	6	±4 dB	±5 dB
13	4	±4 dB	±5 dB
14	2	±5 dB	±6 dB
15	0	±5 dB	±6 dB

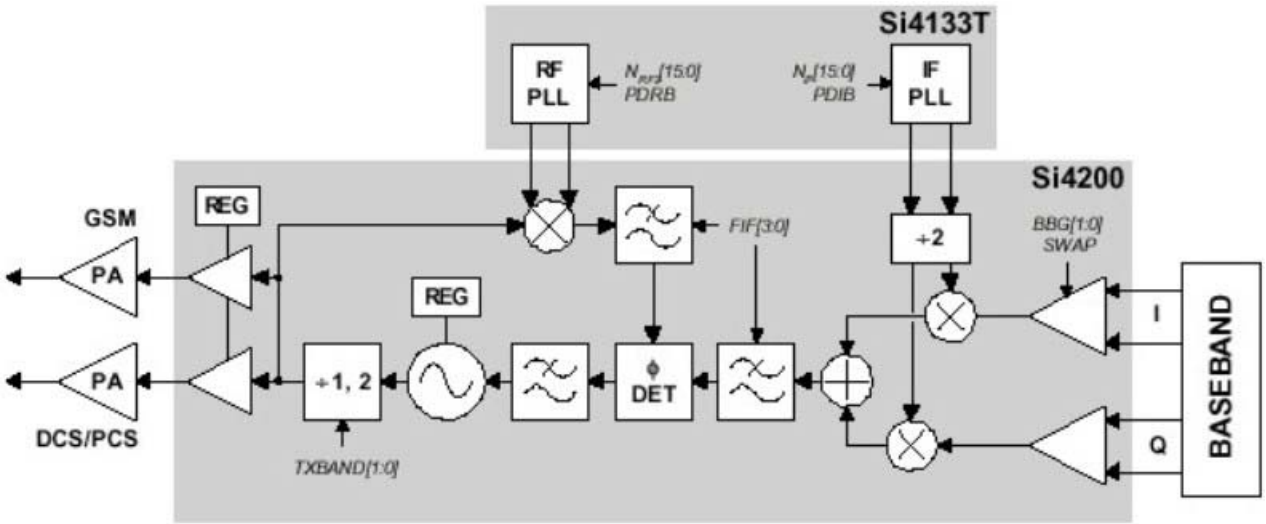


Figure 3-7-4. Transmitter Block Diagram

3.7.4 Antenna Switch module

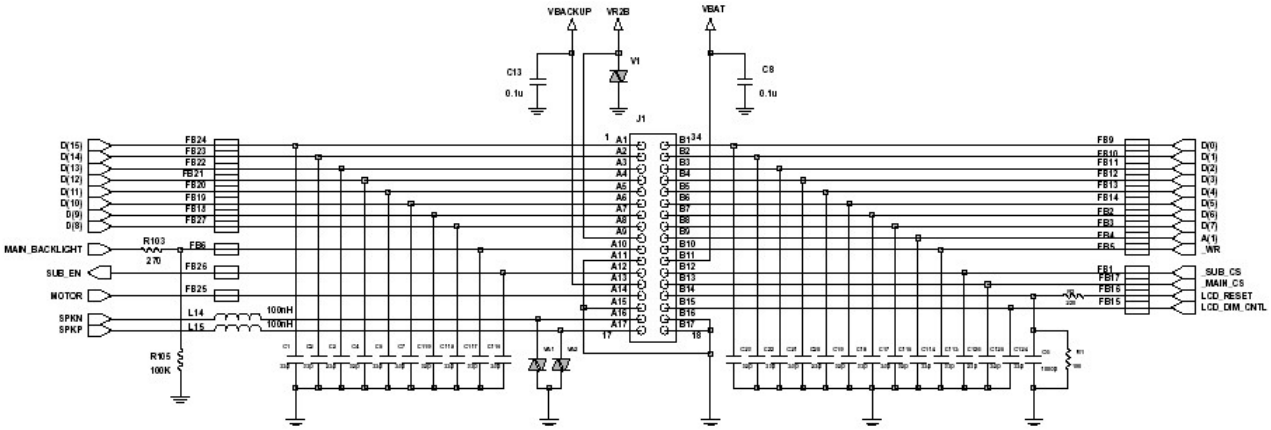
Ant S/W module(LMSP54AA-097) is an antenna switch module for dual band phone.
The logic and current is given below table 1.

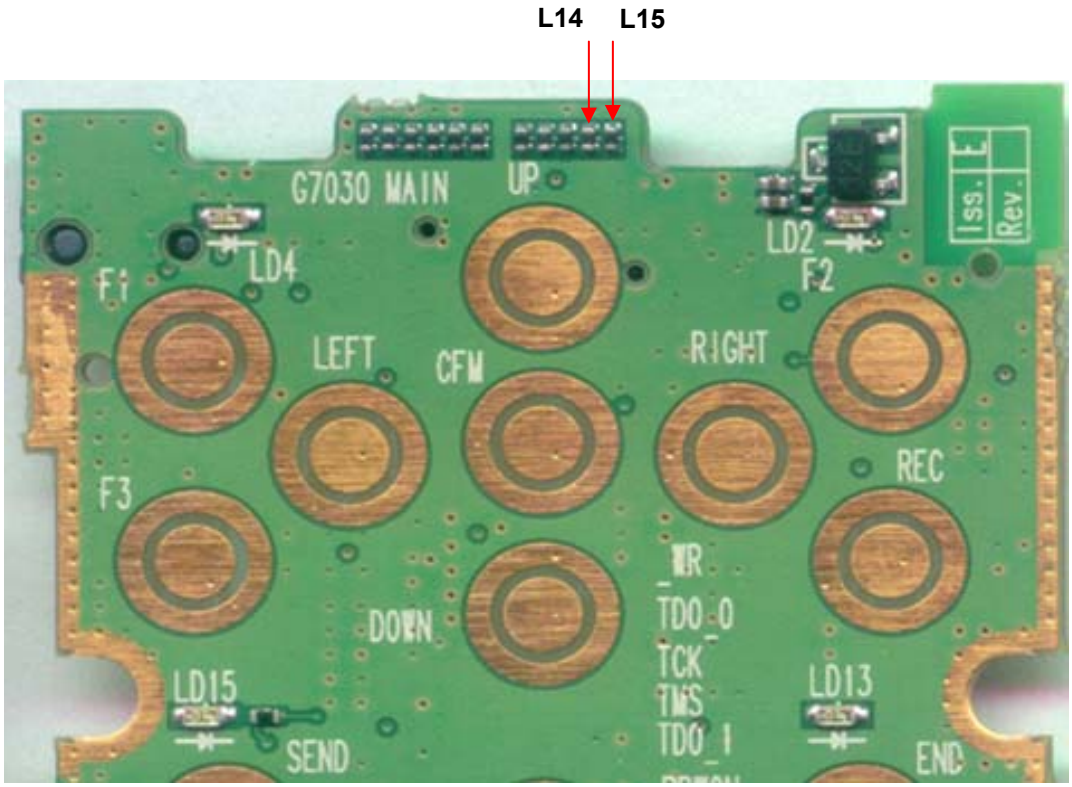
Table 3-7-1 The logic and current

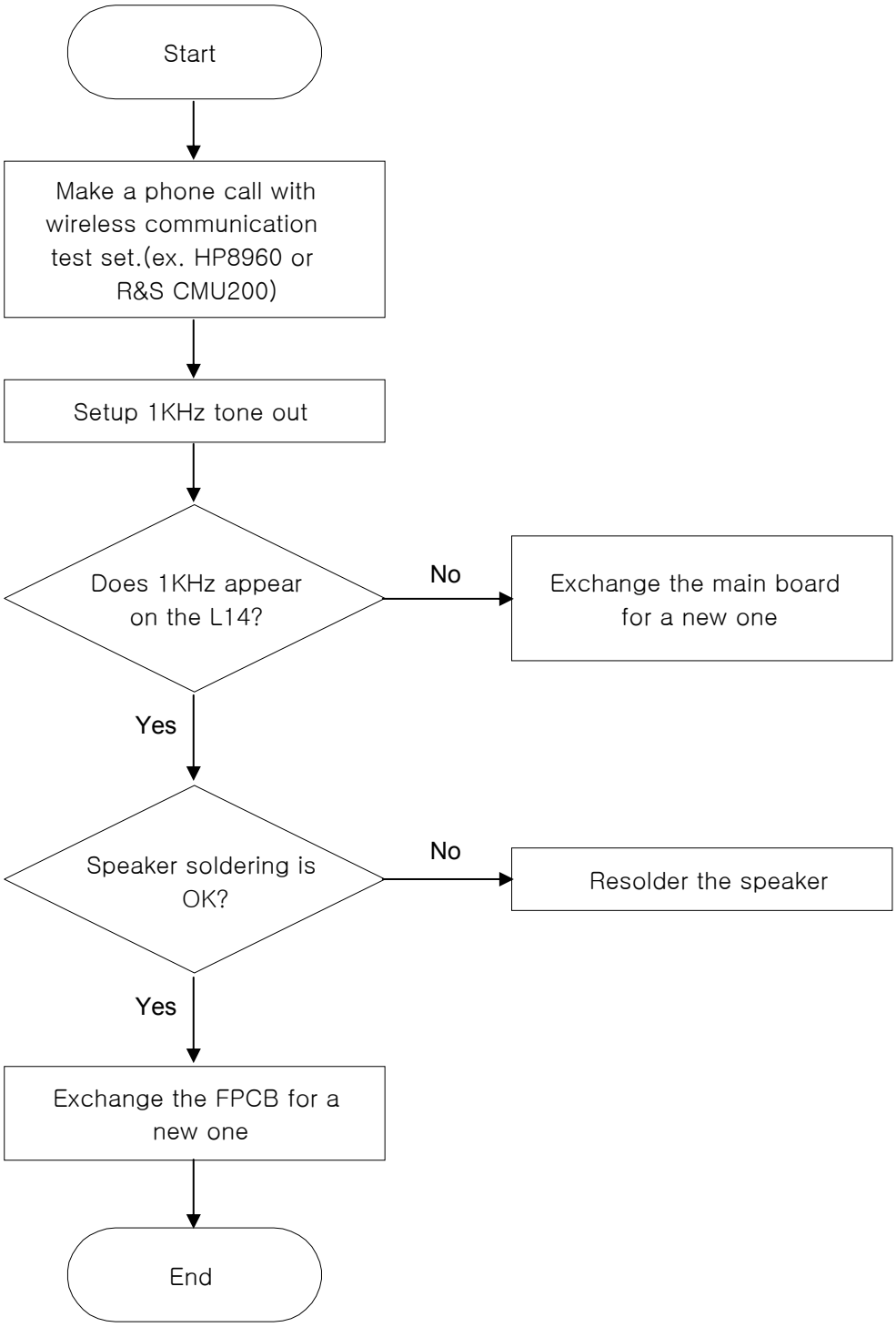
	VC1	VC2	Current
GSM TX	0 V	2.5 ~ 3.0 V	10.0 mA max
DCS TX	2.5 ~ 3.0 V	0 V	10.0 mA max
GSM/DCS RX	0 V	0 V	< 0.1 mA

4. TROUBLE SHOOTING

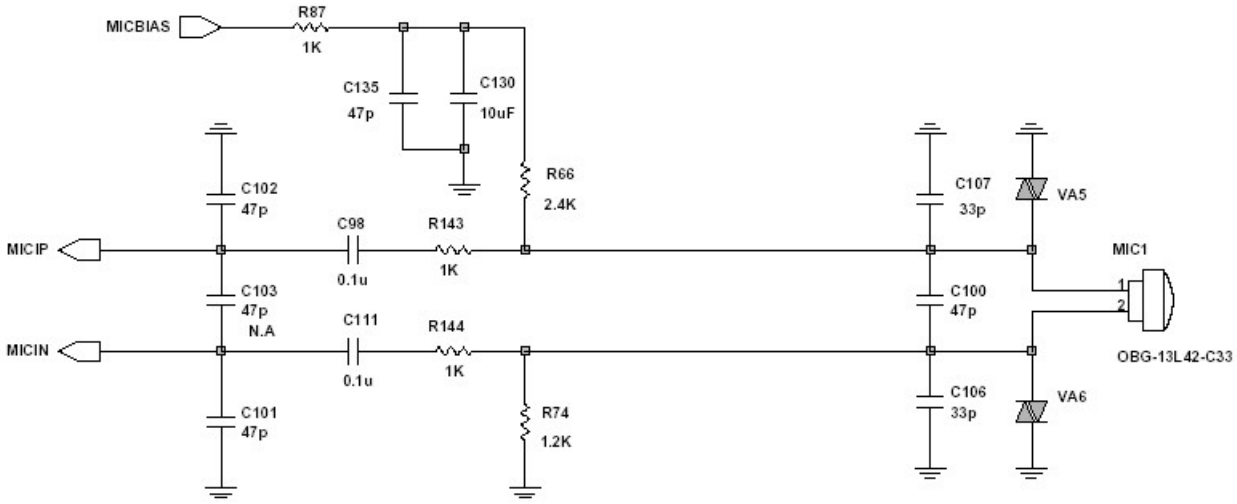
4.1 Speaker

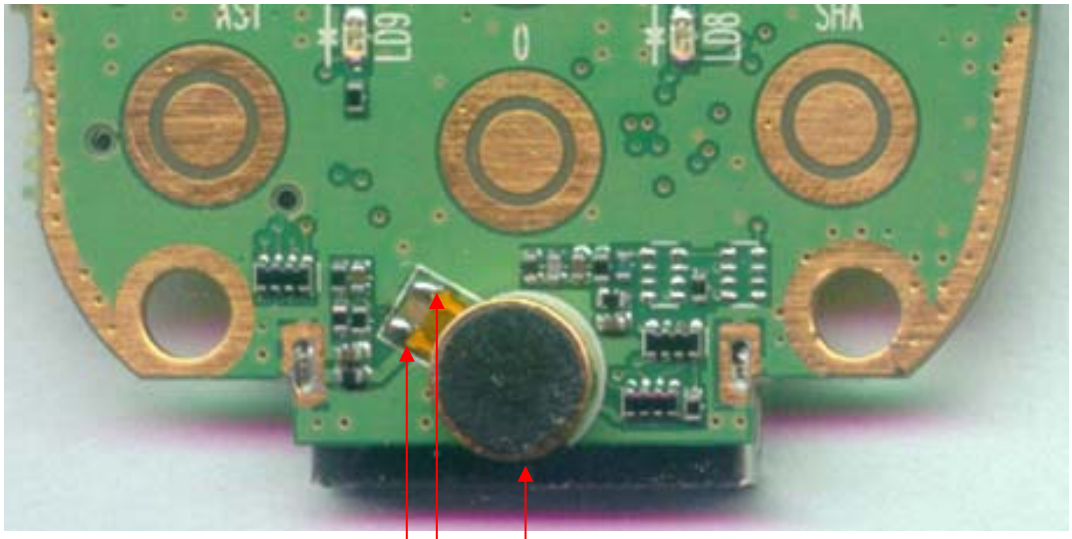





Start
Make a phone call with wireless communication test set.(ex. HP8960 or R&S CMU200)
Setup 1KHz tone out
Does 1KHz appear on the L14?
No
Exchange the main board for a new one
Yes
Speaker soldering is OK?
No
Resolder the speaker
Yes
Exchange the FPCB for a new one
End

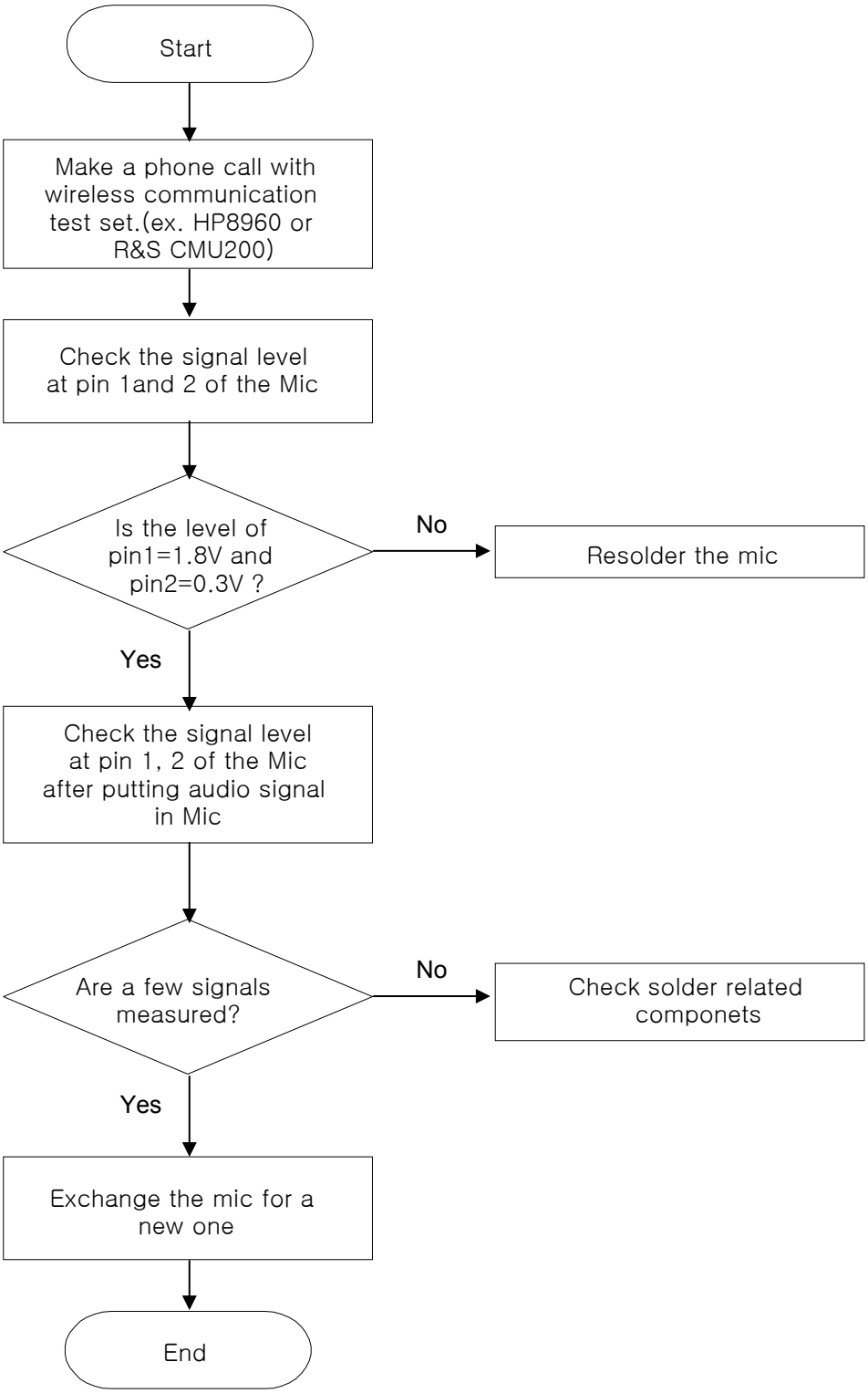
4.2 Microphone



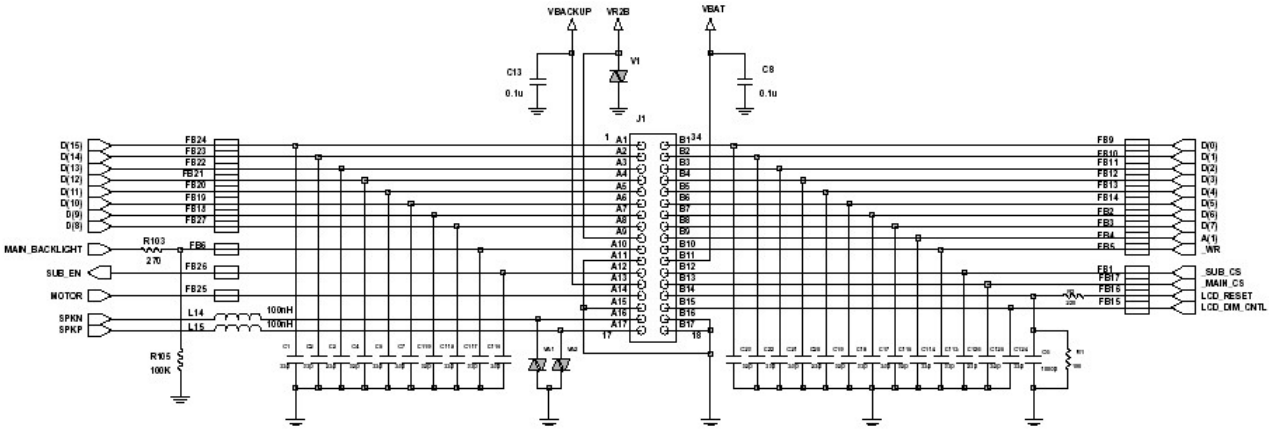


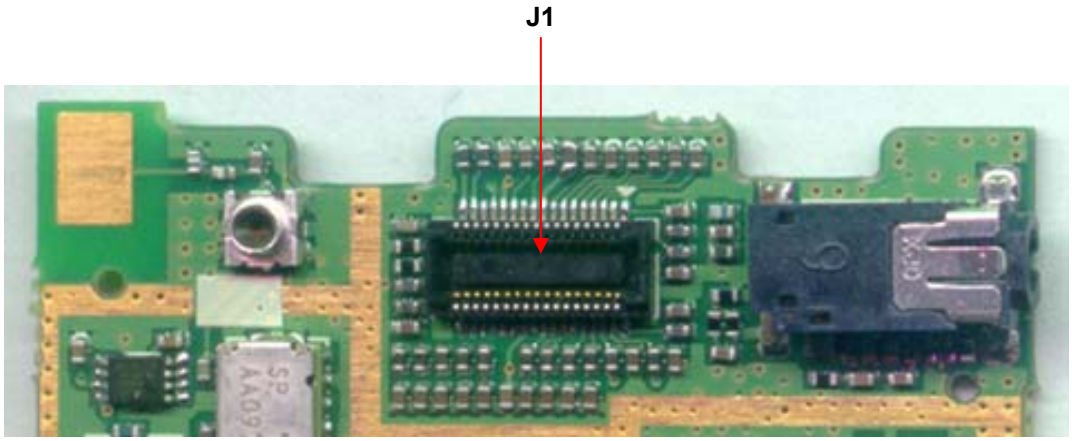
Mic1

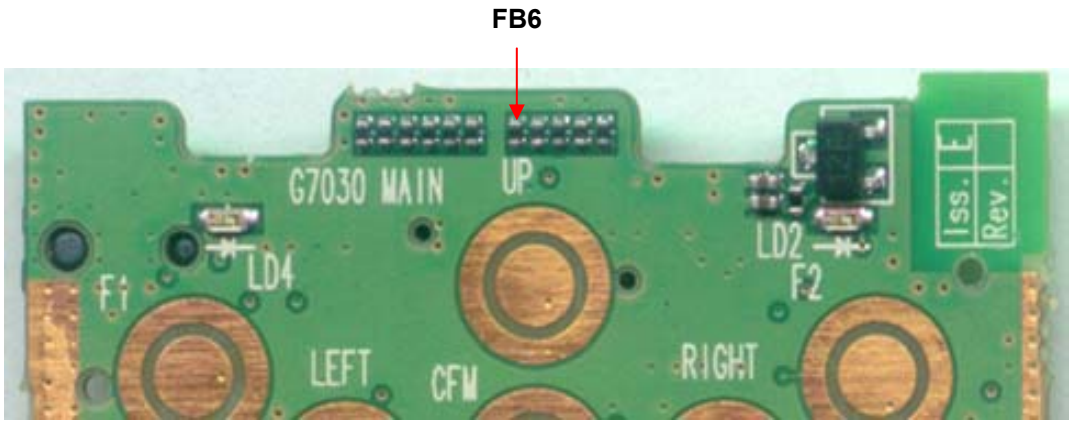
Pin1 Pin2

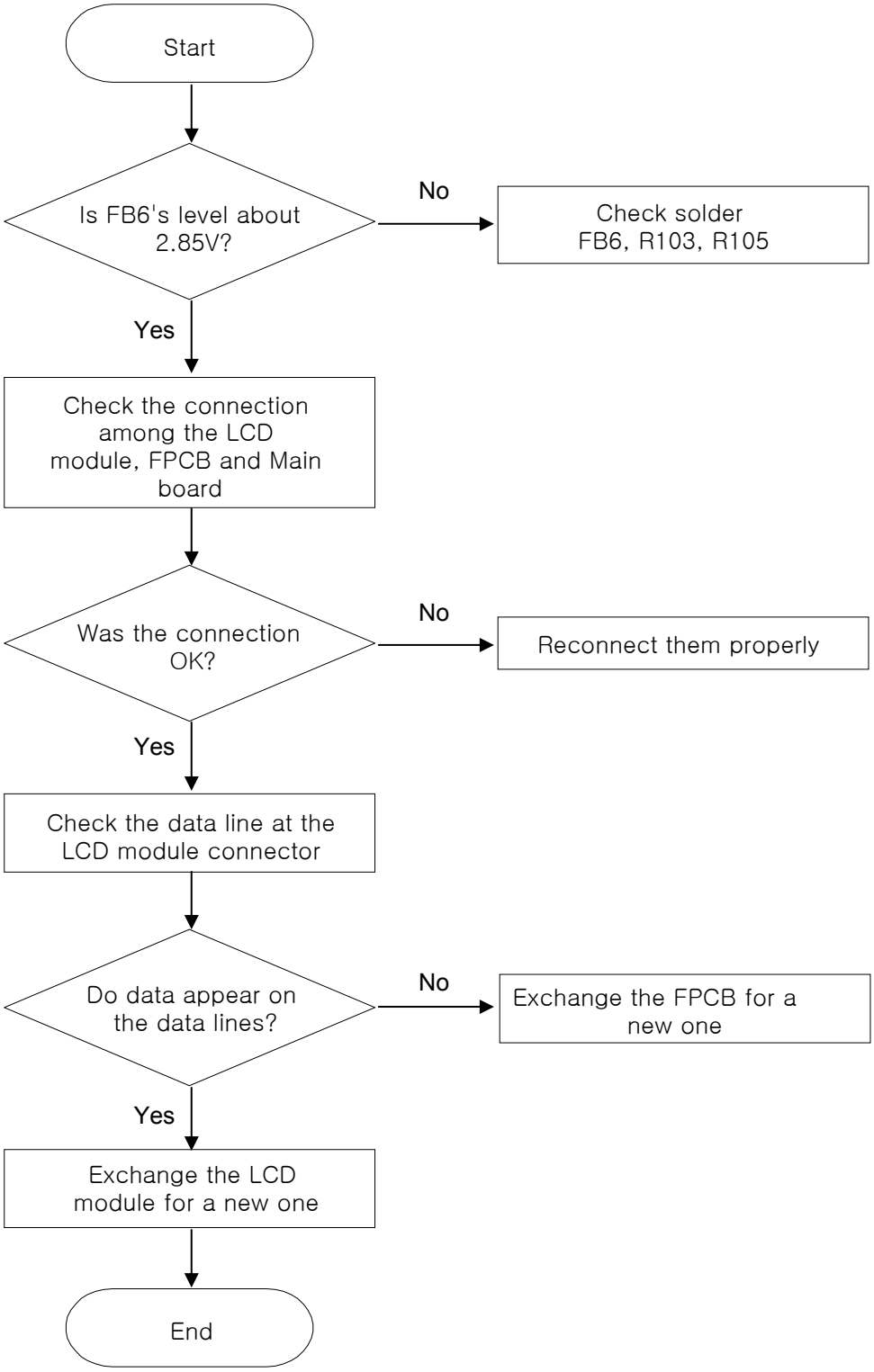

Start
Make a phone call with wireless communication test set.(ex. HP8960 or R&S CMU200)
Check the signal level at pin 1and 2 of the Mic
Is the level of pin1=1.8V and pin2=0.3V ?
No
Resolder the mic
Yes
Check the signal level at pin 1, 2 of the Mic after putting audio signal in Mic
Are a few signals measured?
No
Check solder related componets
Yes
Exchange the mic for a new one
End

4.3 LCD module

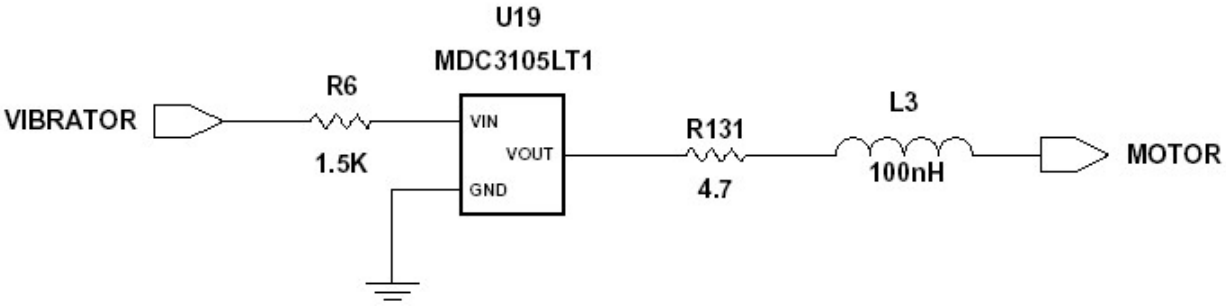


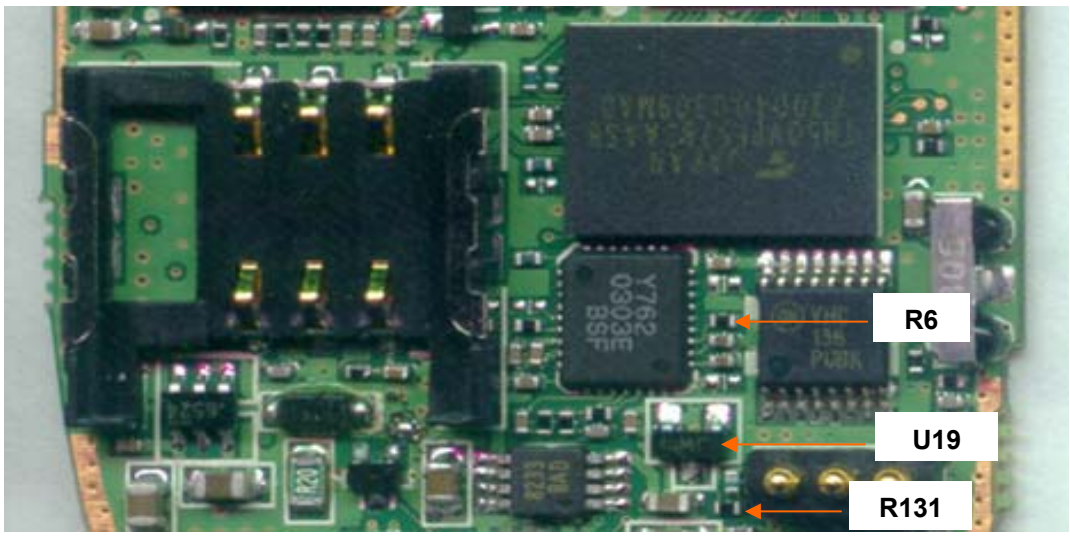


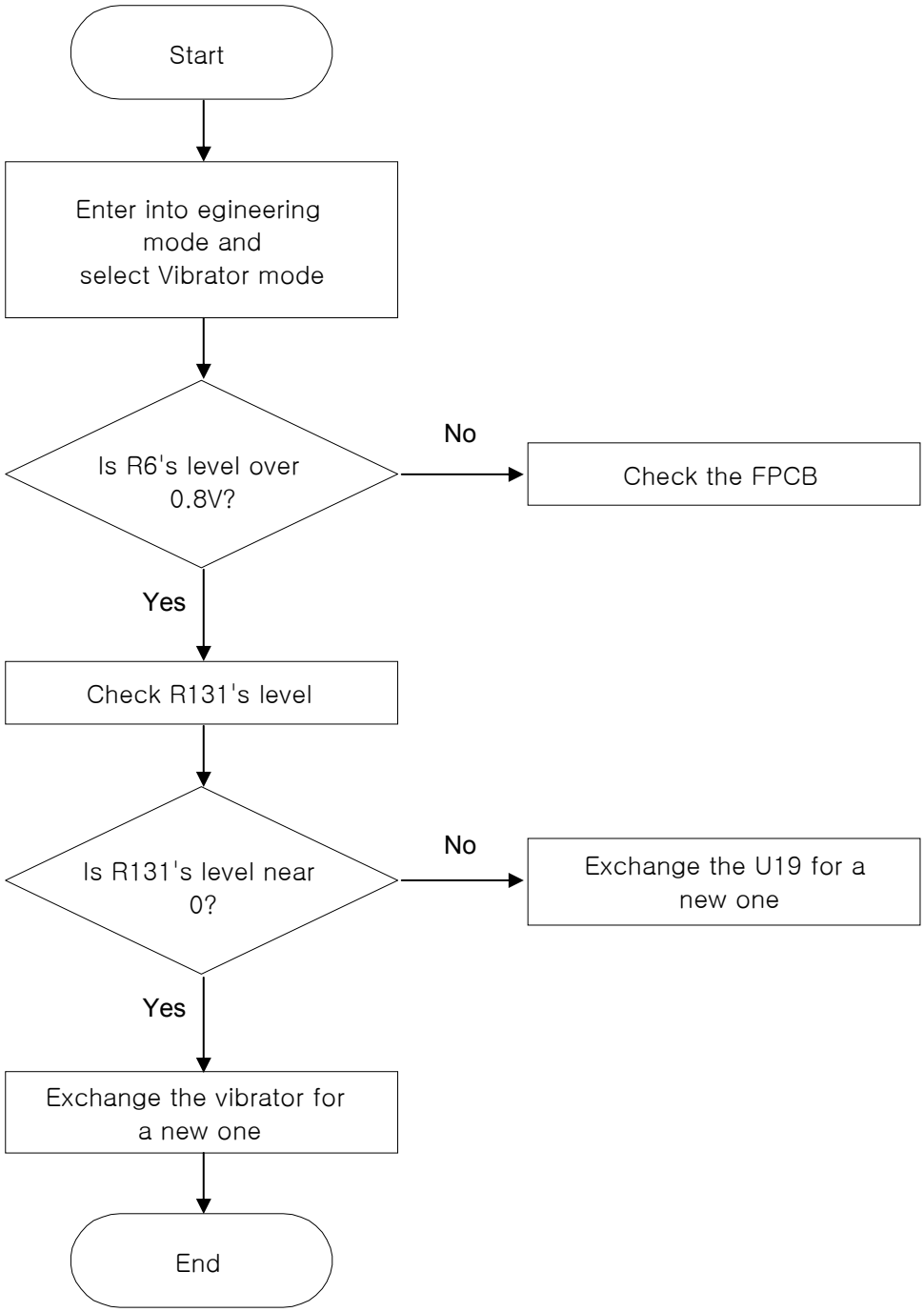



Start
Is FB6's level about 2.85V?
No
Check solder FB6, R103, R105
Yes
Check the connection among the LCD module, FPCB and Main board
Was the connection OK?
No
Reconnect them properly
Yes
Check the data line at the LCD module connector
Do data appear on the data lines?
No
Exchange the FPCB for a new one
Yes
Exchange the LCD module for a new one
End

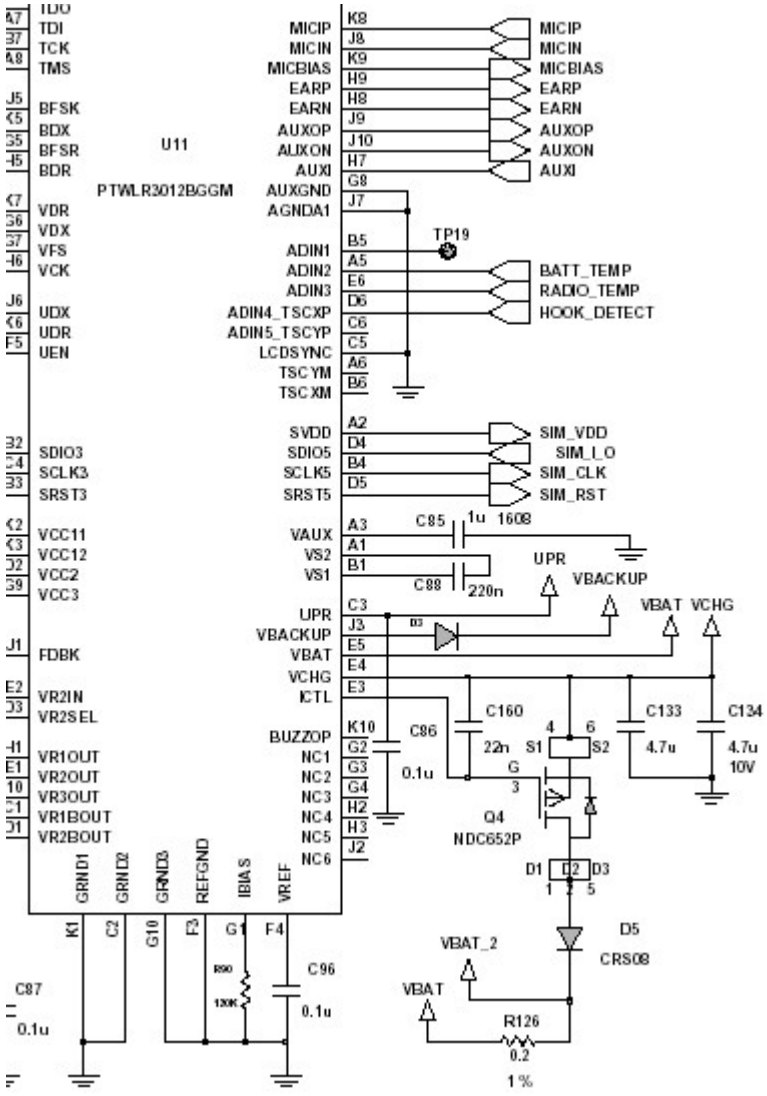
4.4 Vibrator

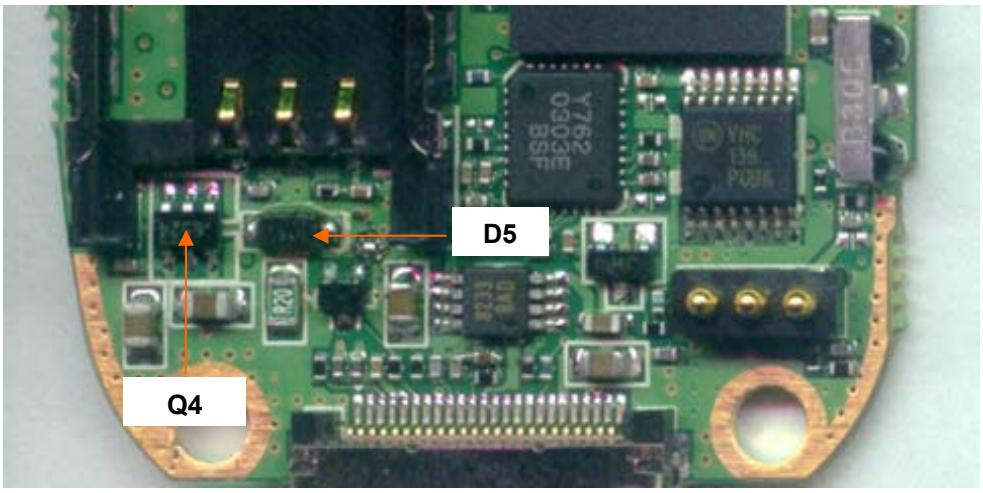

U19
MDC3105LT1
R6
VIBRATOR
1.5K
VIN
VOUT
GND
R131
4.7
L3
100nH
MOTOR

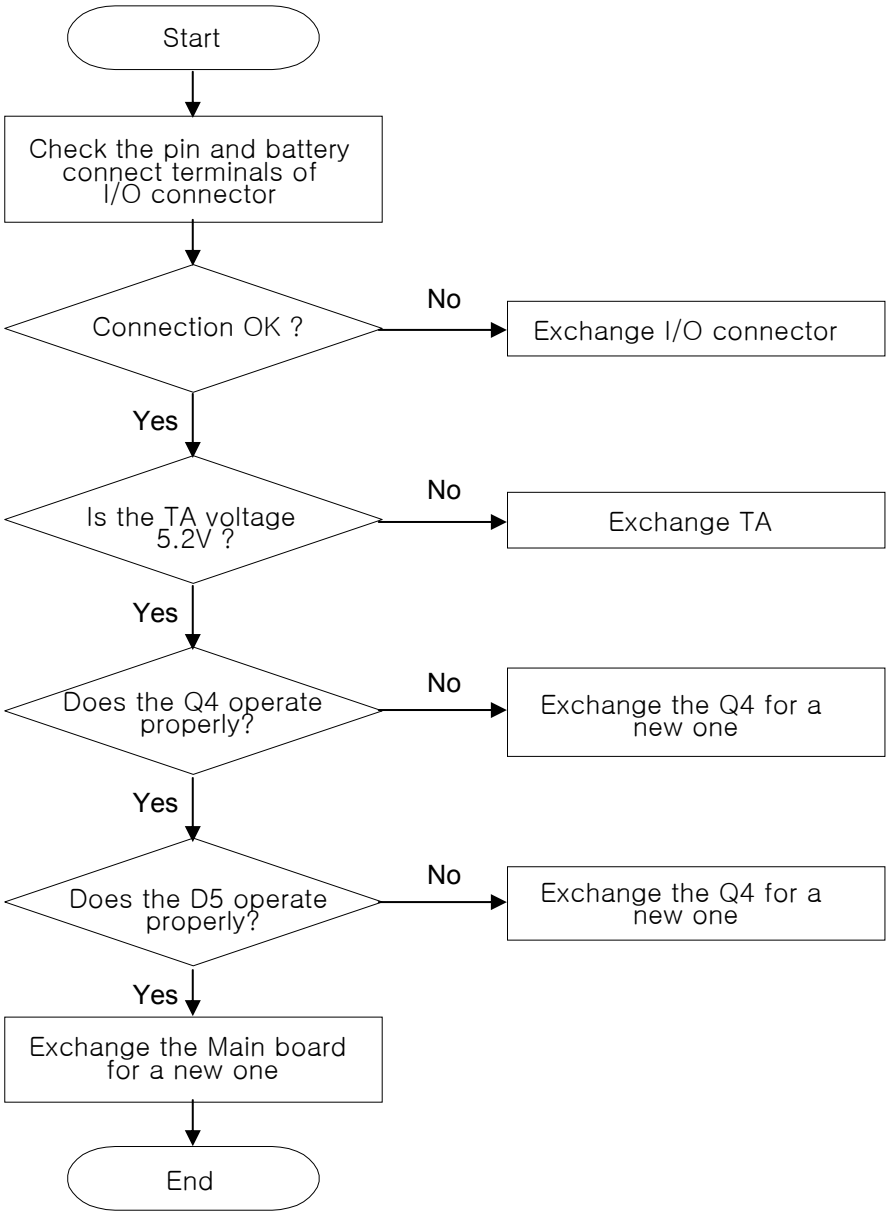

R6
U19
R131


Start
Enter into egineering mode and select Vibrator mode
Is R6's level over 0.8V?
No
Check the FPCB
Yes
Check R131's level
Is R131's level near 0?
No
Exchange the U19 for a new one
Yes
Exchange the vibrator for a new one
End

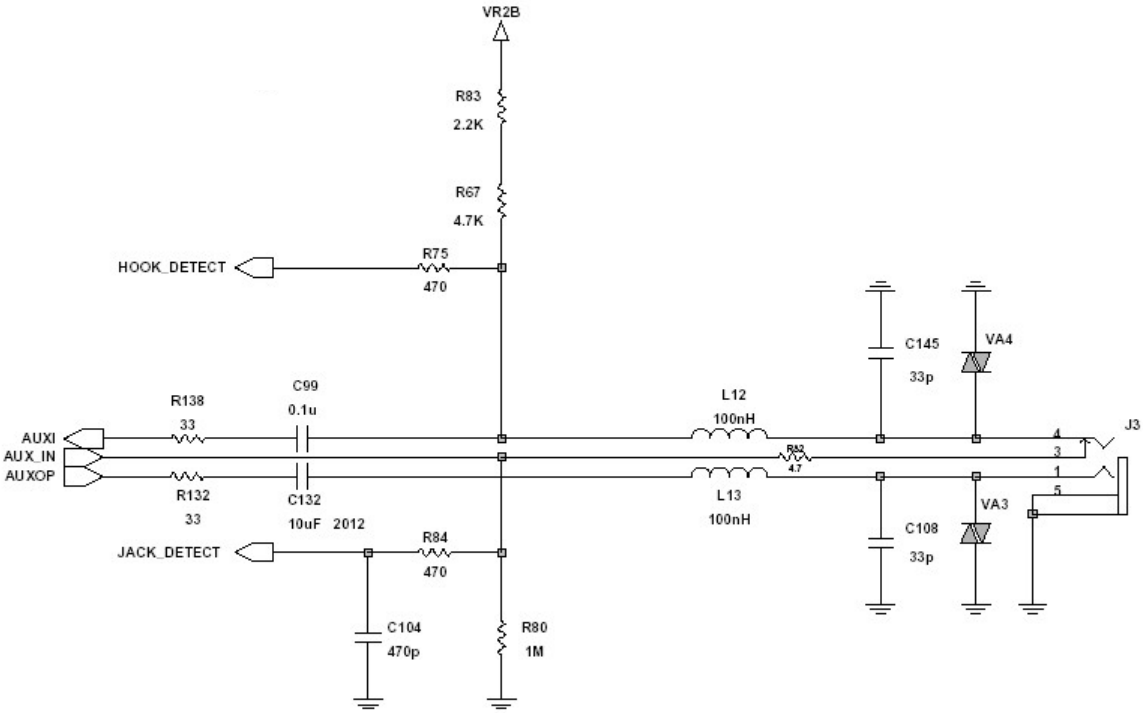
4.5 Charger

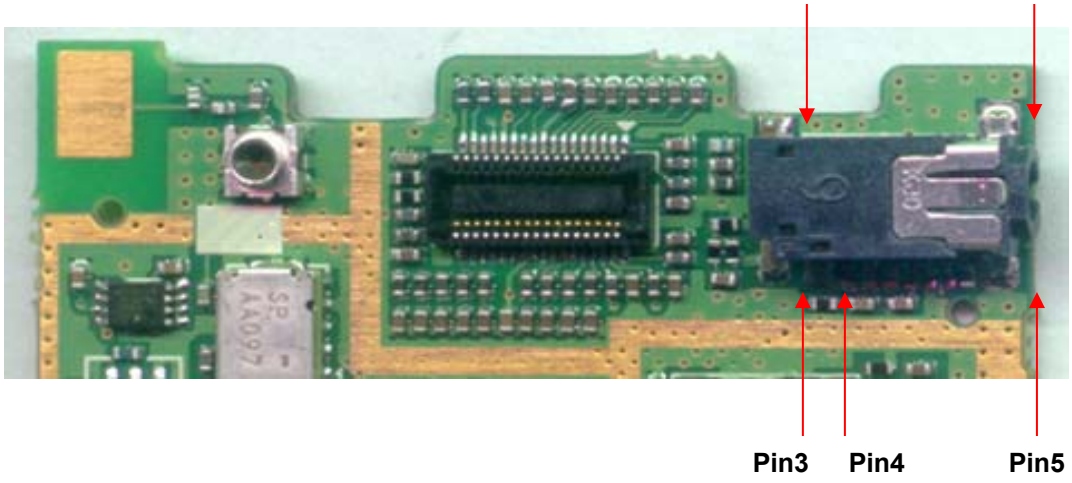

U11
PTWLR3012BGGM
TDI
TCK
TMS
BFSK
BDX
BFSR
BDR
VDR
VDX
VFS
VCK
UDX
UDR
UEN
SDIO3
SCLK3
SRST3
VCC11
VCC12
VCC2
VCC3
FDBK
VR2IN
VR2SEL
VR1OUT
VR2OUT
VR3OUT
VR1BOUT
VR2BOUT
GRND1
GRND2
GRND3
REFGND
IBIAS
VREF
MICIP
MICIN
MICBIAS
EARP
EARN
AUXOP
AUXON
AUXI
AUXGND
AGNDA1
ADIN1
ADIN2
ADIN3
ADIN4_TSCXP
ADIN5_TSCYP
LCDSYNC
TSCYM
TSCXM
SVDD
SDIO5
SCLK5
SRST5
VAUX
VS2
VS1
UPR
VBACKUP
VBAT
VCHG
ICTL
BUZZOP
NC1
NC2
NC3
NC4
NC5
NC6
TP19
BATT_TEMP
RADIO_TEMP
HOOK_DETECT
SIM_VDD
SIM_I_O
SIM_CLK
SIM_RST
C85
1u
1608
C88
220n
C86
0.1u
C160
22n
C87
0.1u
C96
0.1u
R90
130K
S1
S2
G
Q4
NDC652P
C133
4.7u
C134
4.7u
10V
D1
D2
D3
D5
CRS08
VBAT_2
R126
0.2
1%

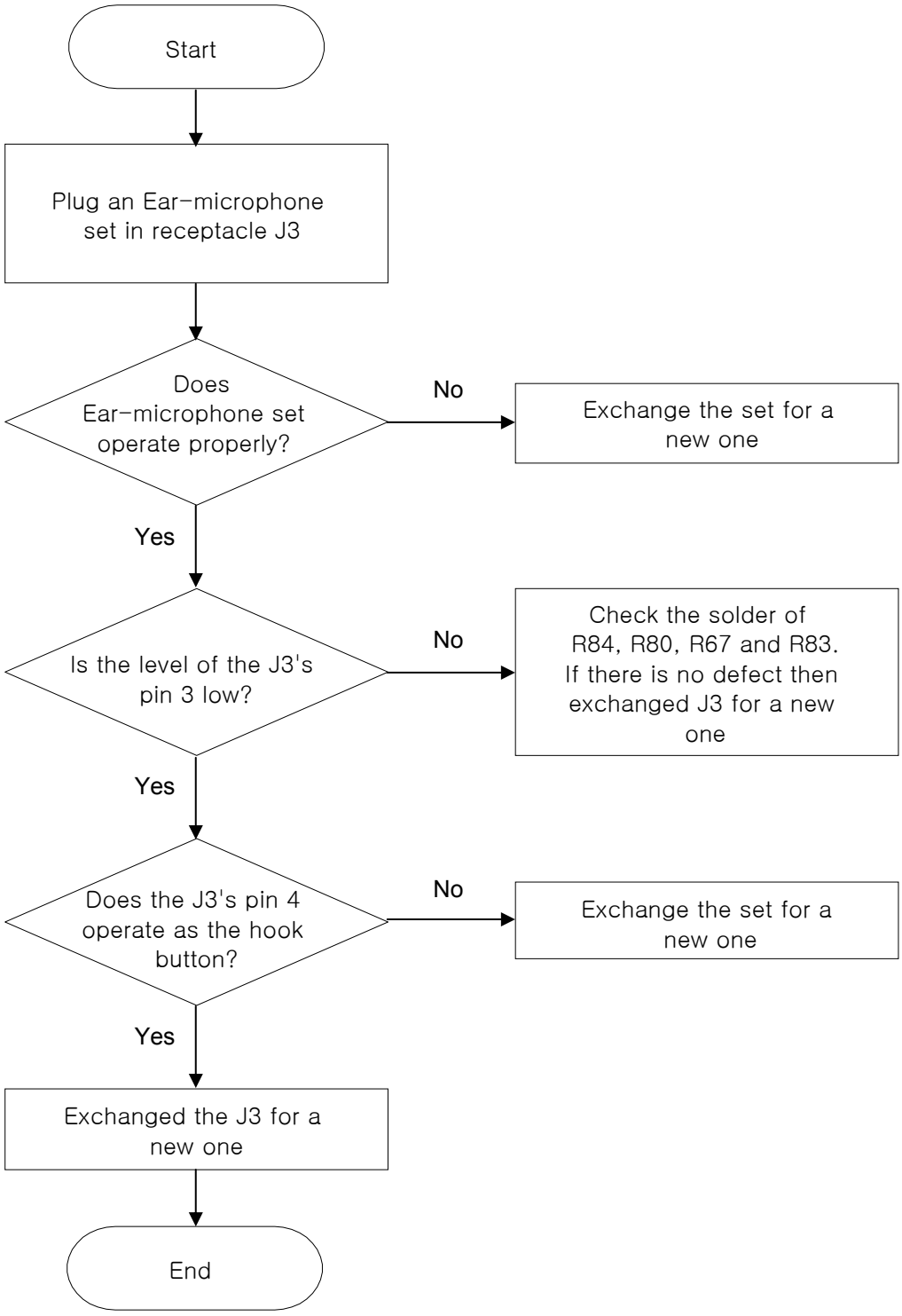

D5
Q4


Start
Check the pin and battery connect terminals of I/O connector
Connection OK ?
No
Exchange I/O connector
Yes
Is the TA voltage 5.2V ?
No
Exchange TA
Yes
Does the Q4 operate properly?
No
Exchange the Q4 for a new one
Yes
Does the D5 operate properly?
No
Exchange the Q4 for a new one
Yes
Exchange the Main board for a new one
End

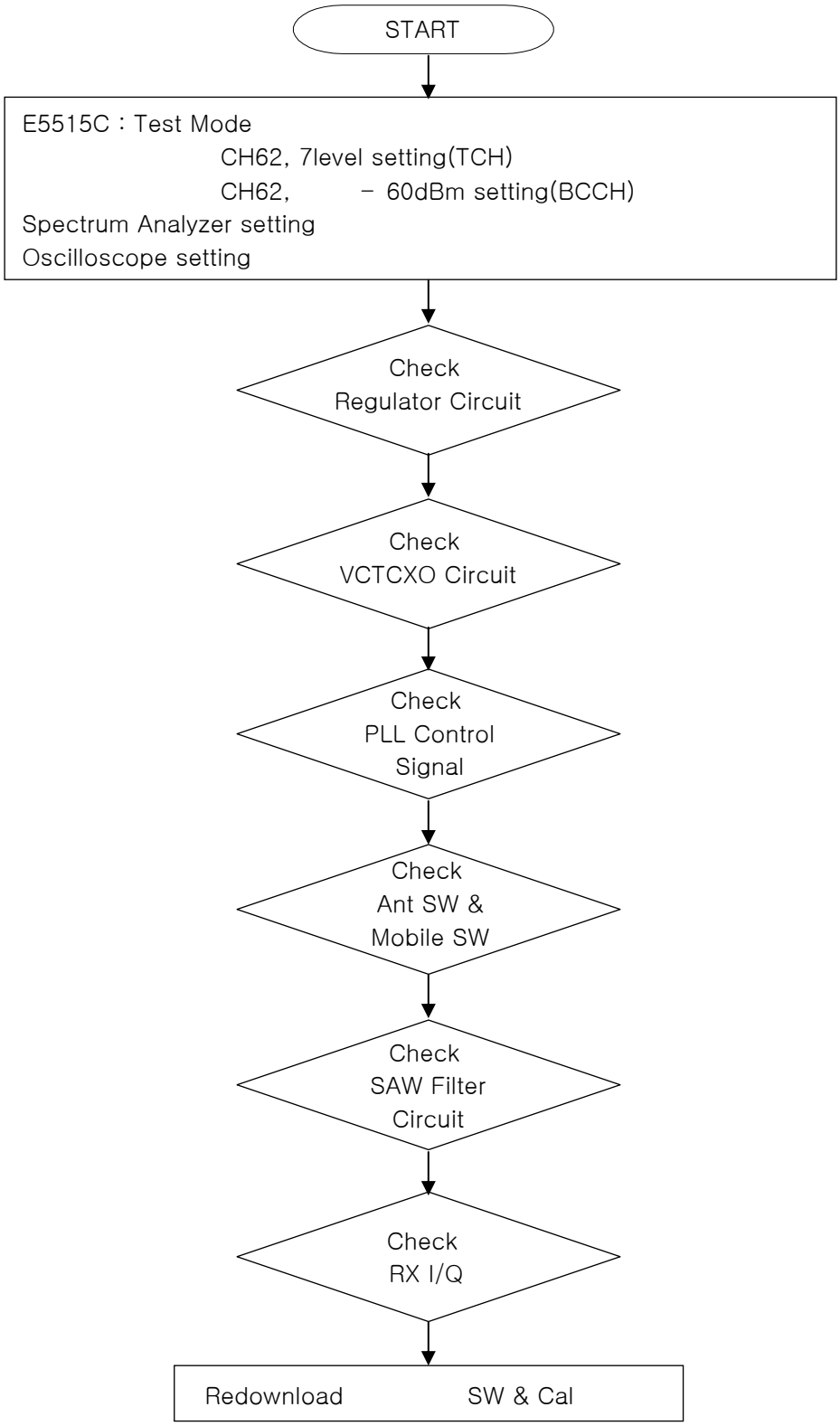
4.6 Ear-Jack


VR2B
R83
2.2K
R67
4.7K
HOOK_DETECT
R75
470
C145
33p
VA4
R138
33
C99
0.1u
L12
100nH
J3
AUXI
AUX_IN
AUXOP
R132
33
C132
10uF 2012
L13
100nH
VA3
C108
33p
JACK_DETECT
R84
470
C104
470p
R80
1M

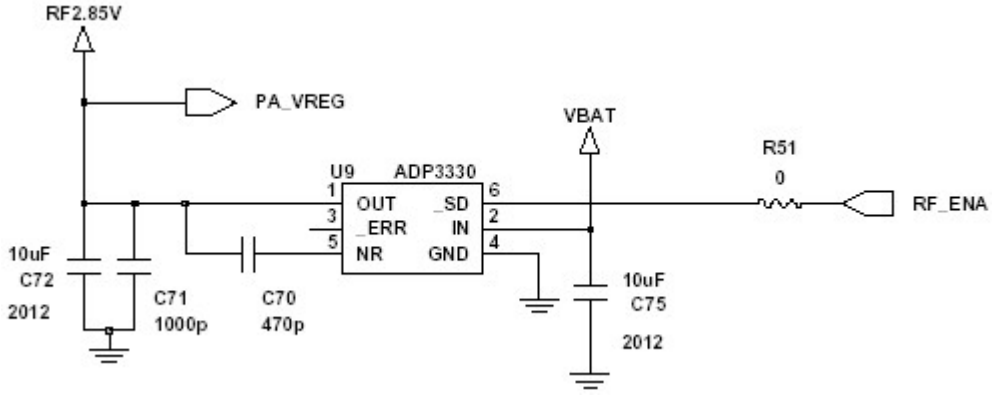

Pin1
Pin2
Pin3
Pin4
Pin5

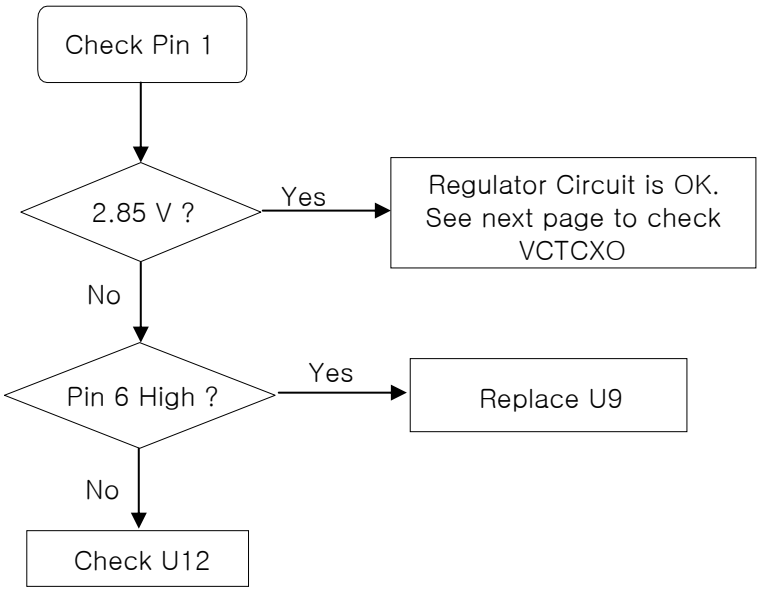

Start
Plug an Ear-microphone set in receptacle J3
Does Ear-microphone set operate properly?
No
Exchange the set for a new one
Yes
Is the level of the J3's pin 3 low?
No
Check the solder of R84, R80, R67 and R83. If there is no defect then exchanged J3 for a new one
Yes
Does the J3's pin 4 operate as the hook button?
No
Exchange the set for a new one
Yes
Exchanged the J3 for a new one
End

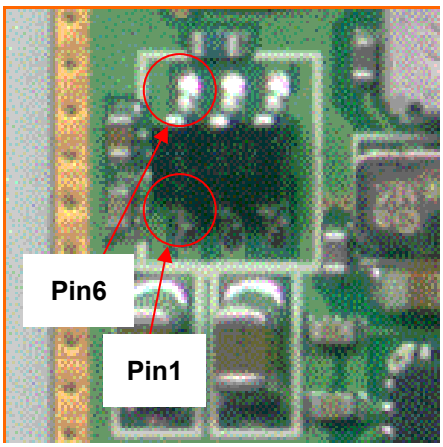
4.7 Rx Path Trouble Shooting

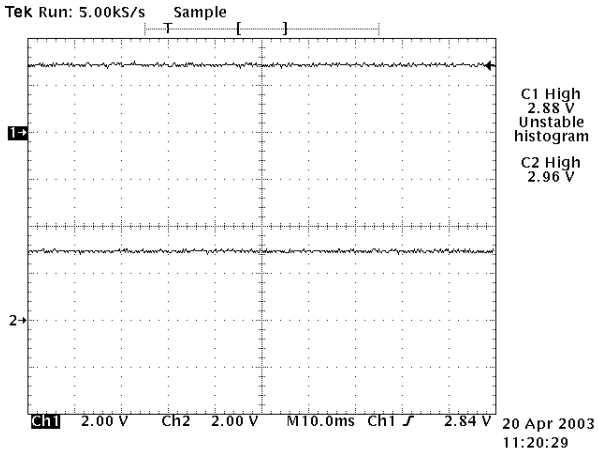


4.7.1 Checking Regulator Circuit

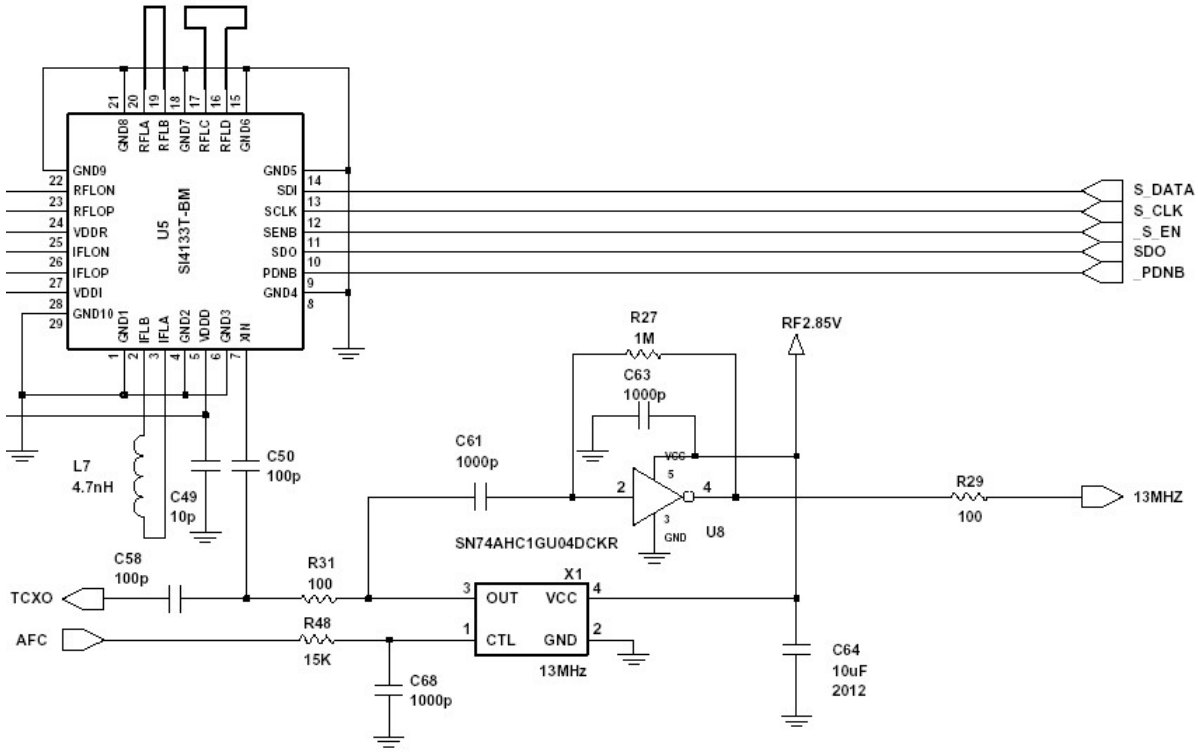


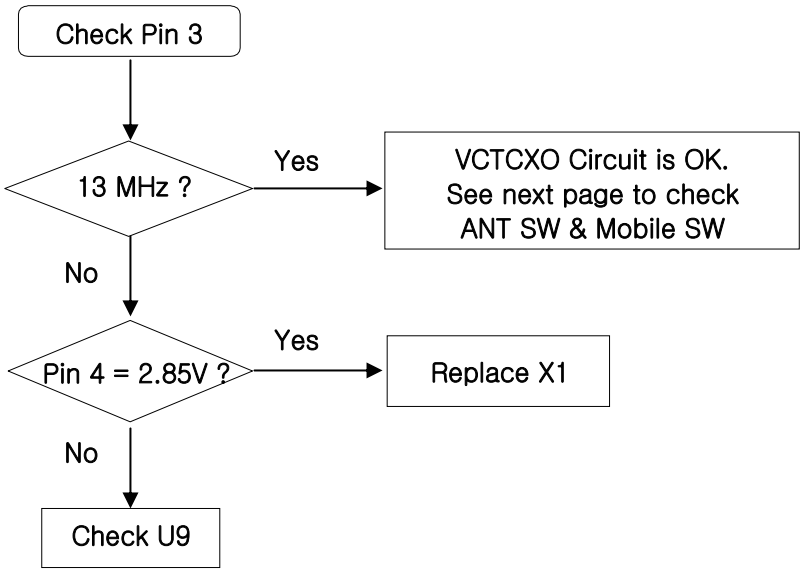


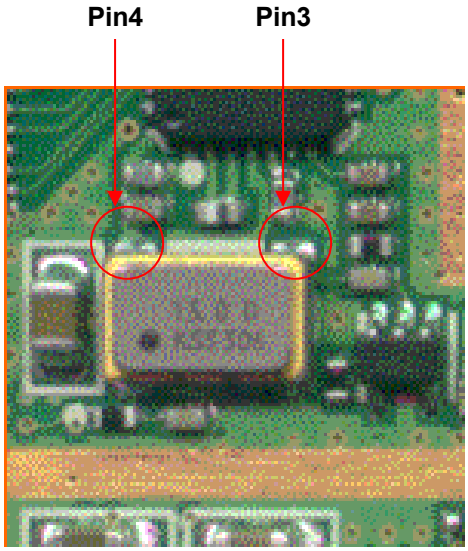


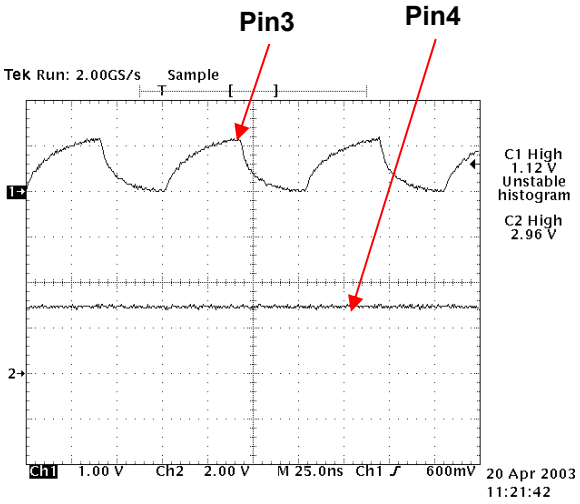


4.7.2 Checking VCTCXO Circuit

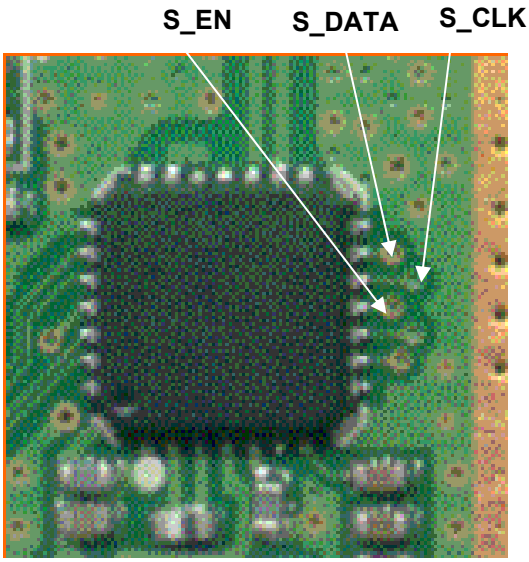


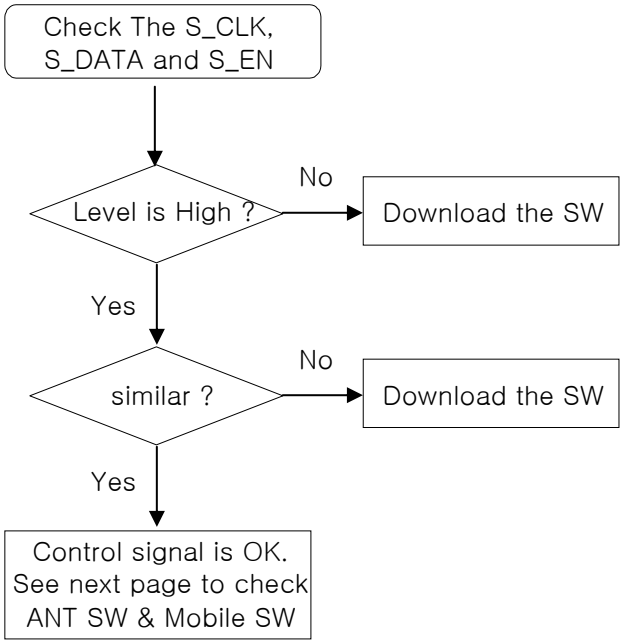


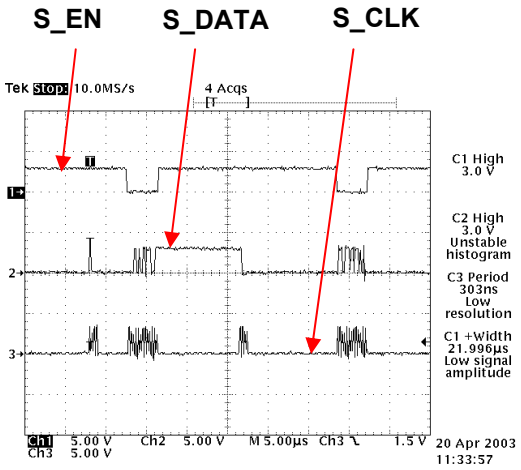

Pin4
Pin3

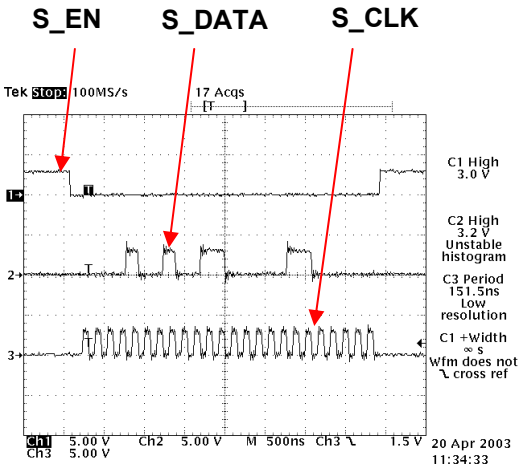

Pin3
Pin4
Tek Run: 2.00GS/s Sample
C1 High
1.12 V
Unstable
histogram
C2 High
2.96 V
Ch1 1.00 V Ch2 2.00 V M 25.0ns Ch1 600mV
20 Apr 2003
11:21:42

4.7.3 Checking PLL Circuit

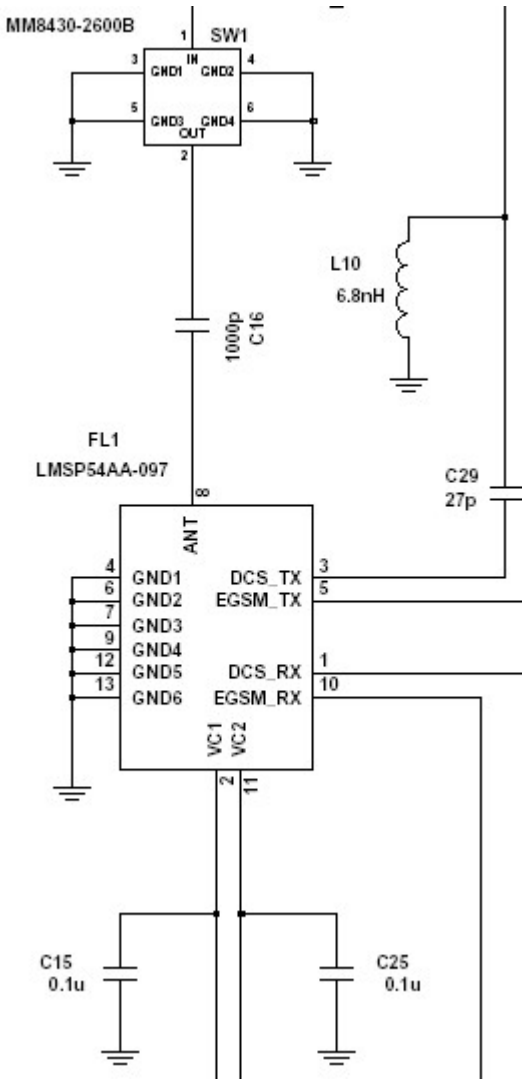


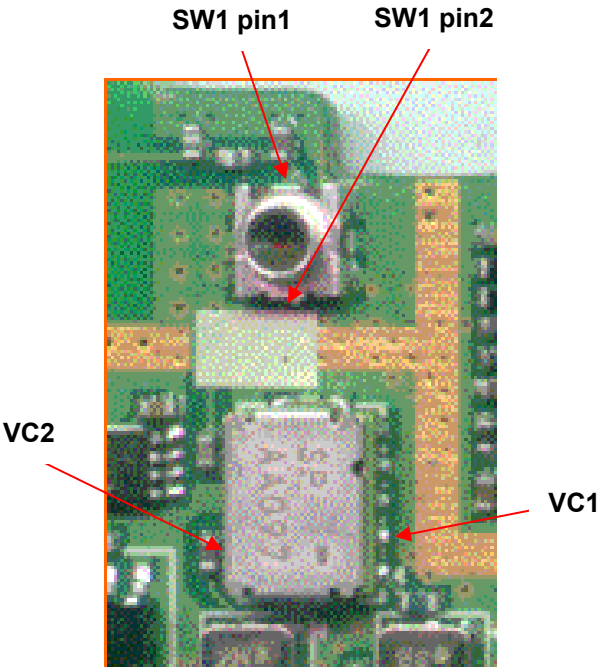


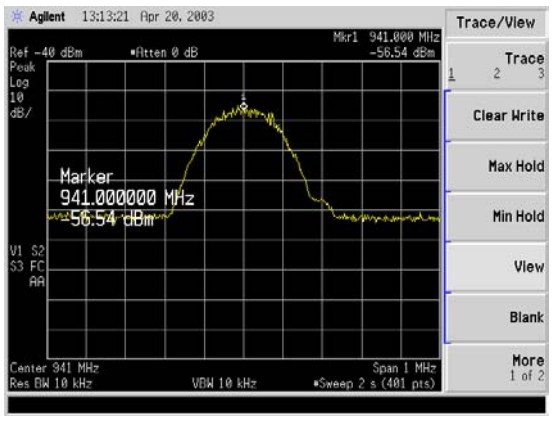


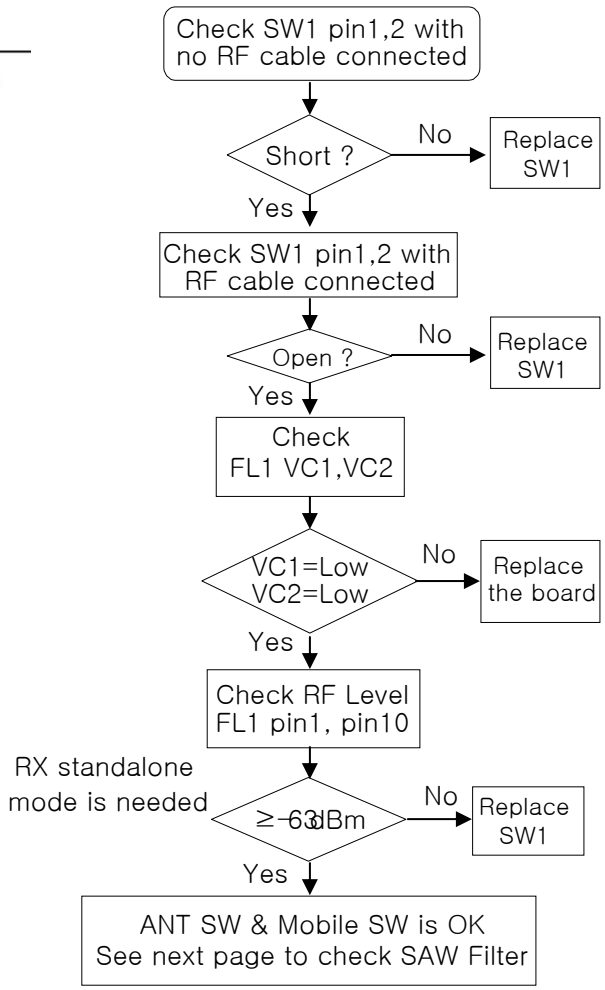


4.7.4 Checking ANT SW & Mobile SW

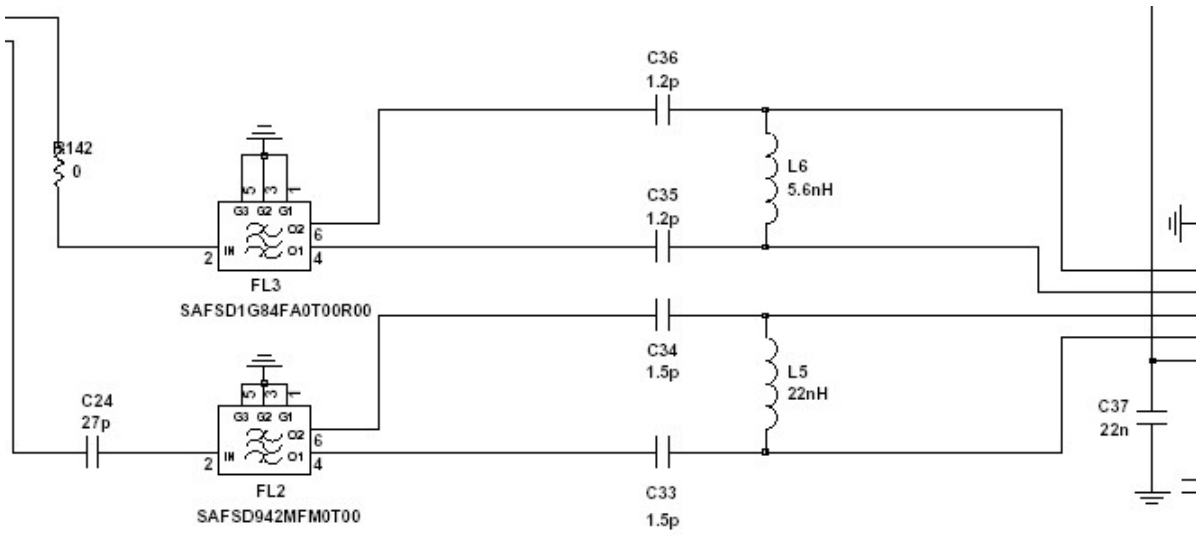


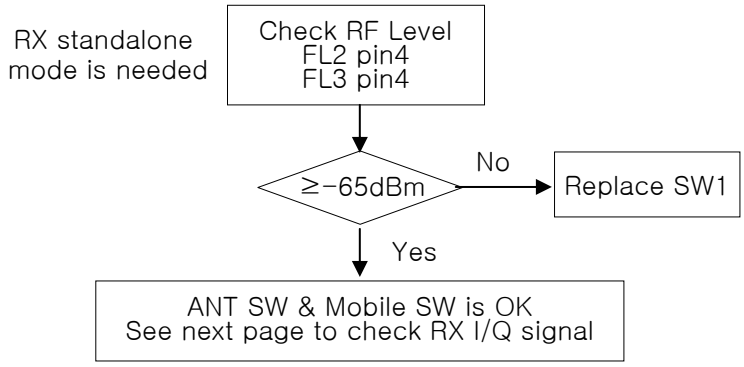




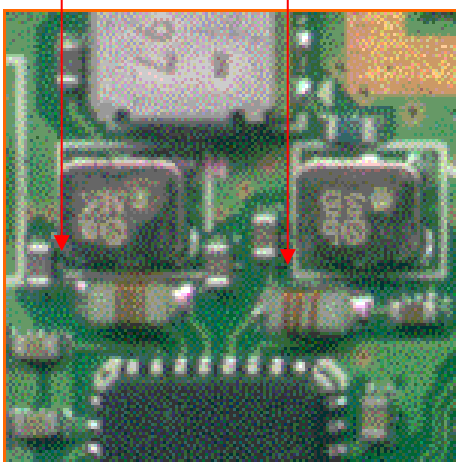


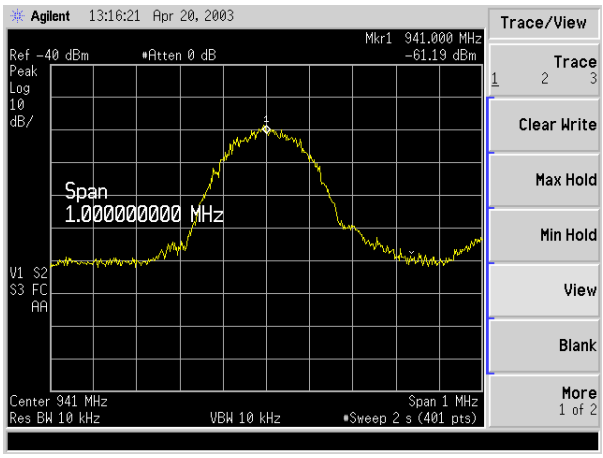
4.7.5 Checking SAW Filter Circuit



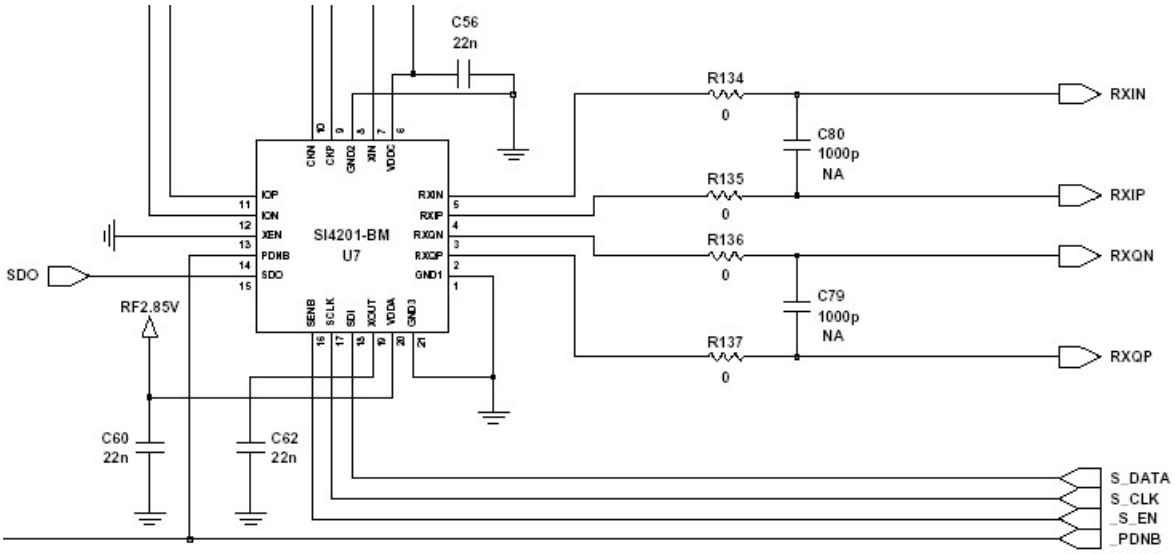


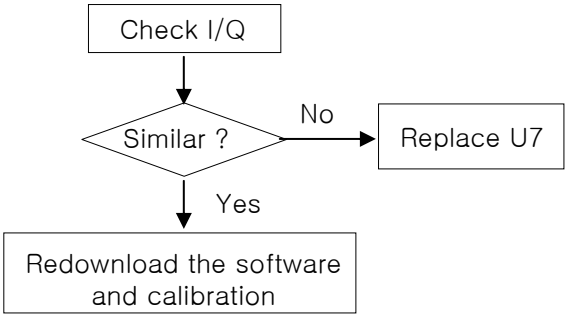
FL2 pin4 **FL3 pin4**

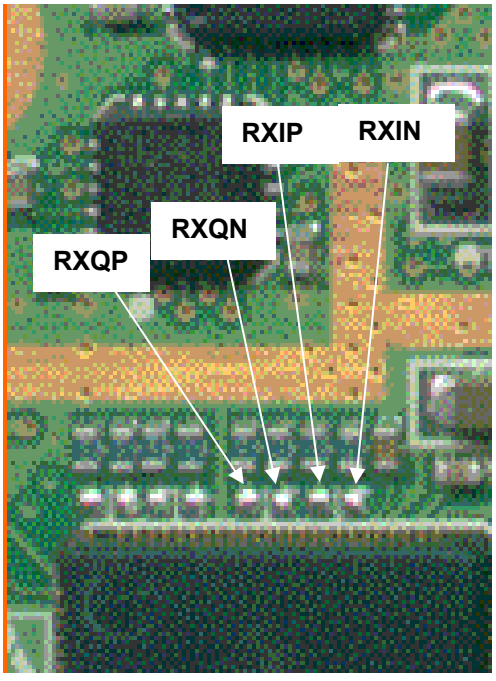


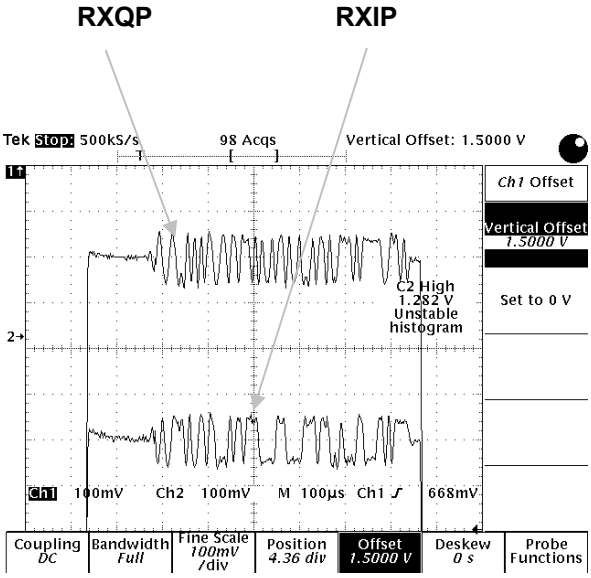


4.7.6 Checking RX I/Q

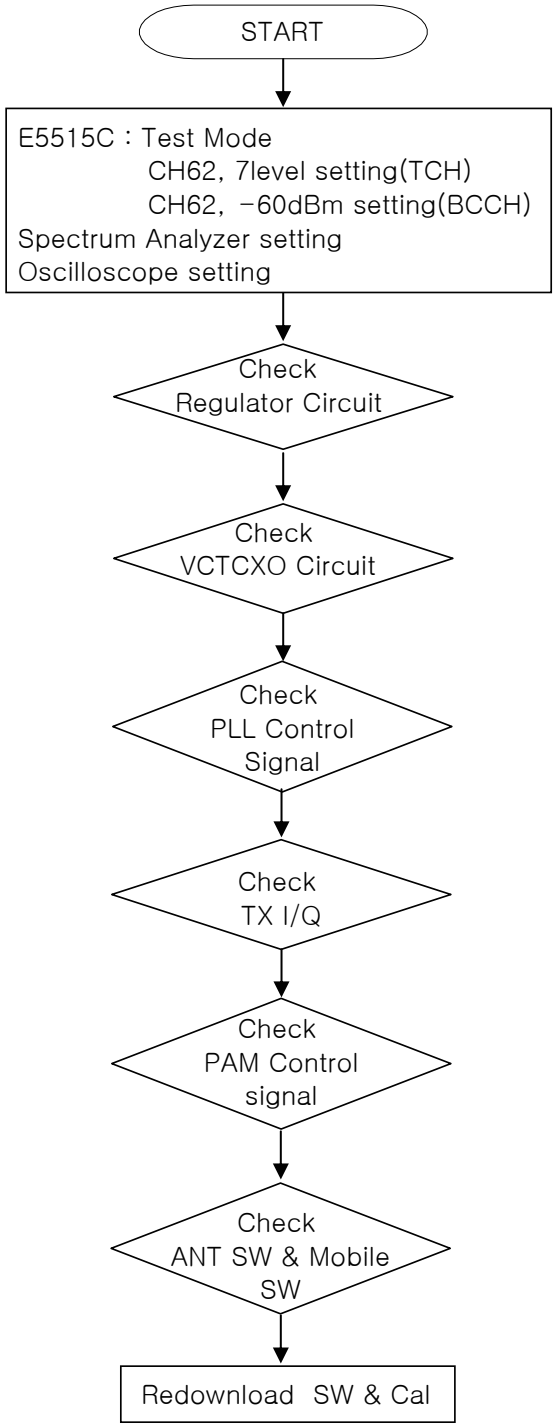




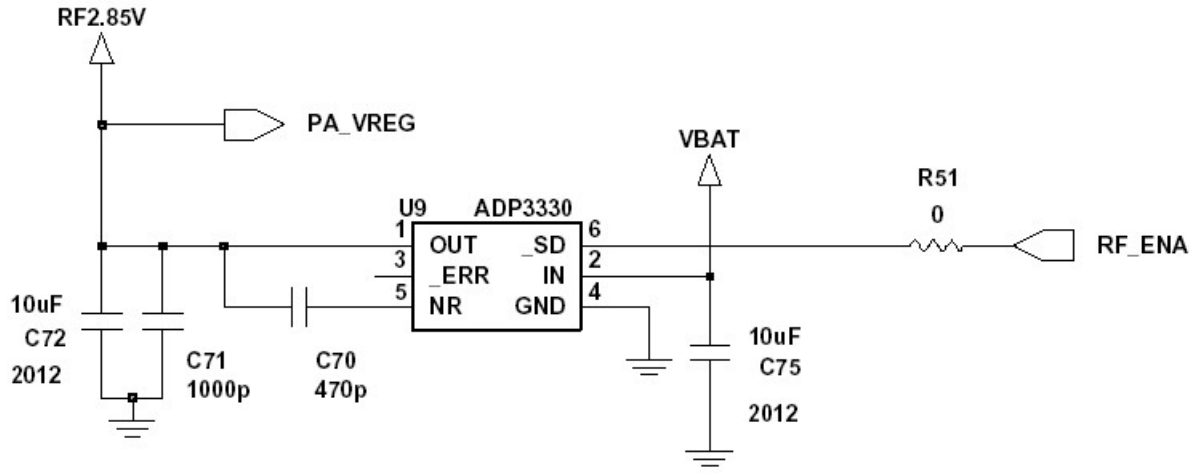


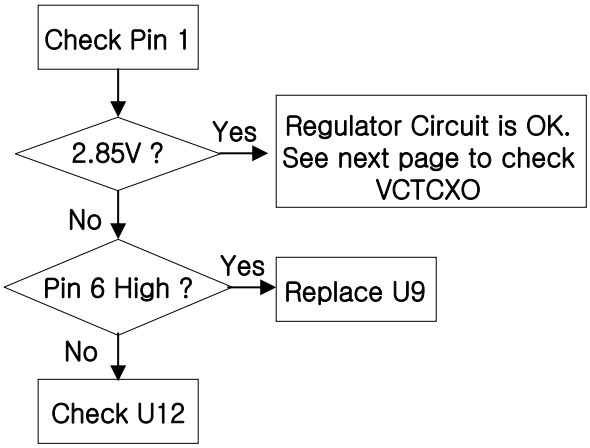


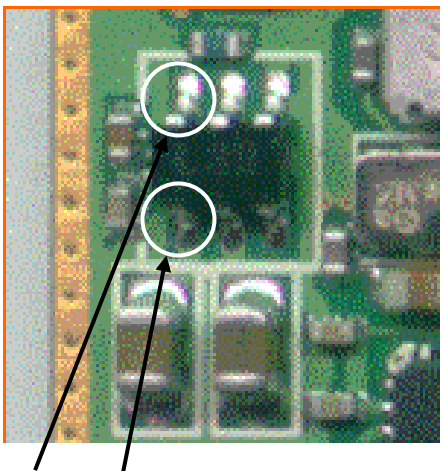
4.8 Tx Path Trouble Shooting

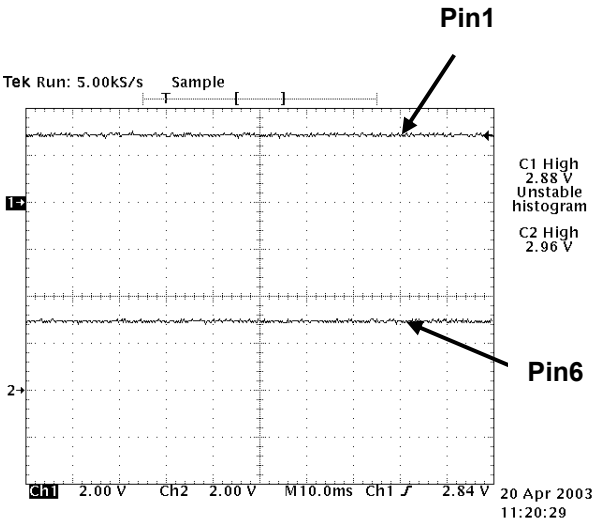


4.8.1 Checking Regulator Circuit

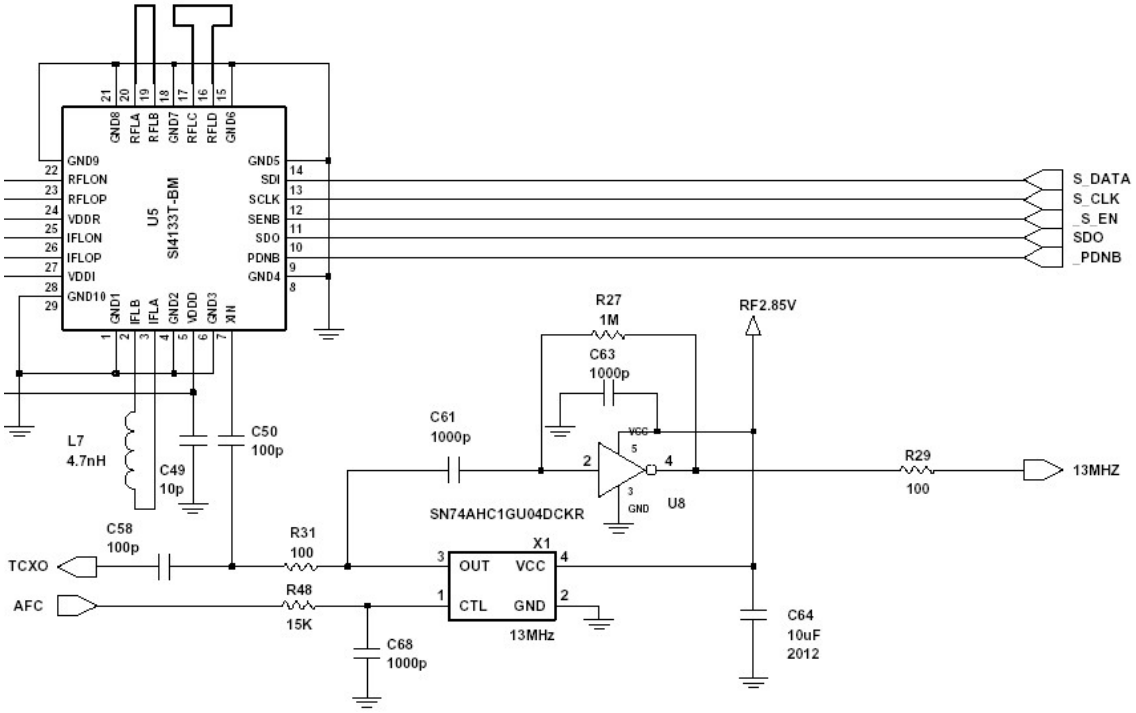


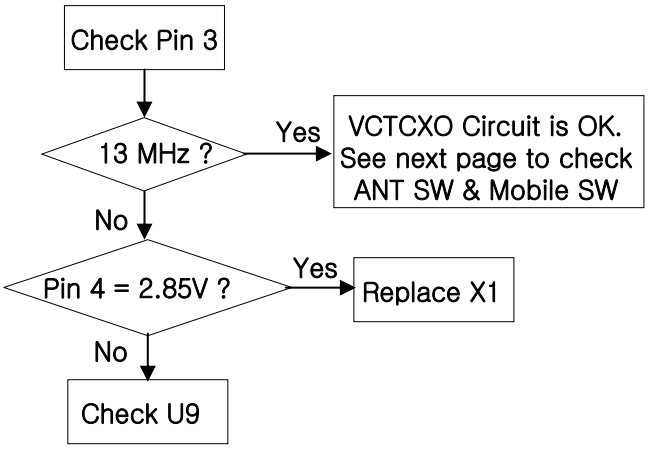


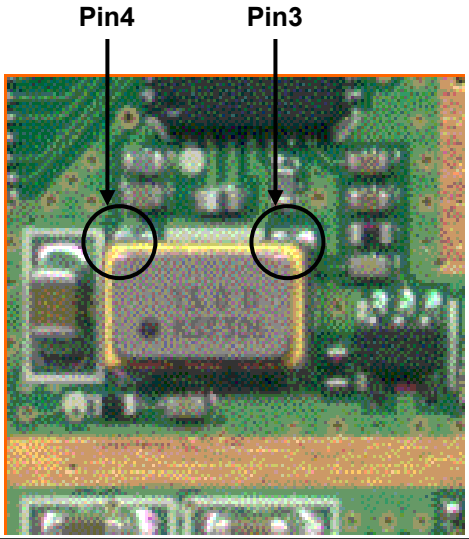


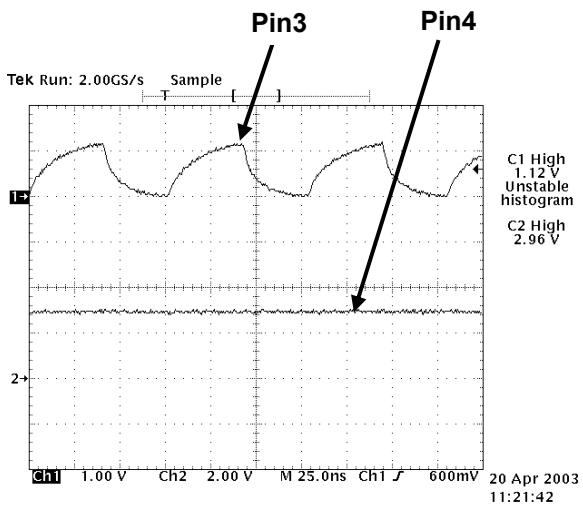


4.8.2 Checking VCTCXO Circuit

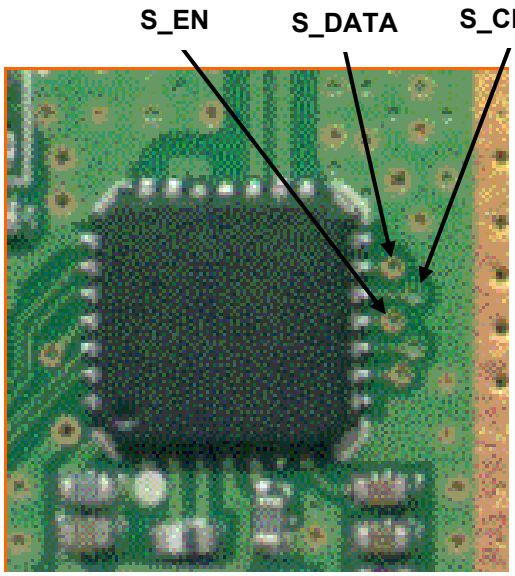


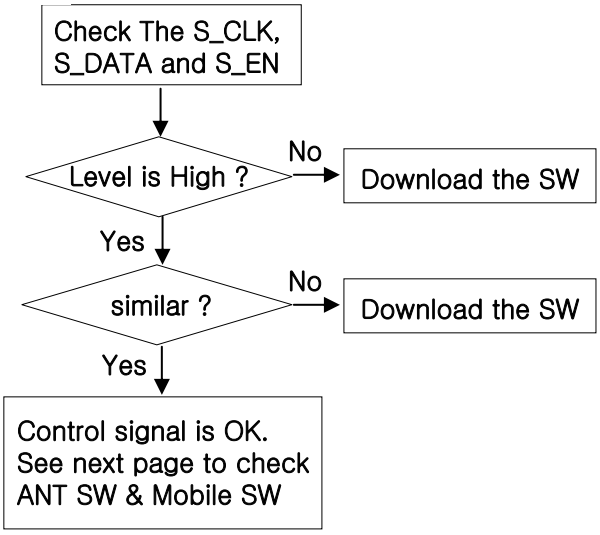


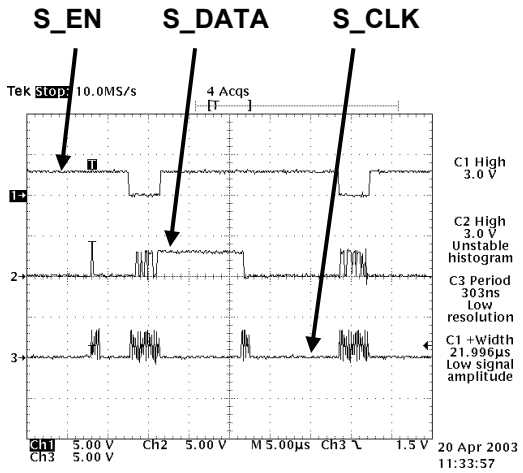


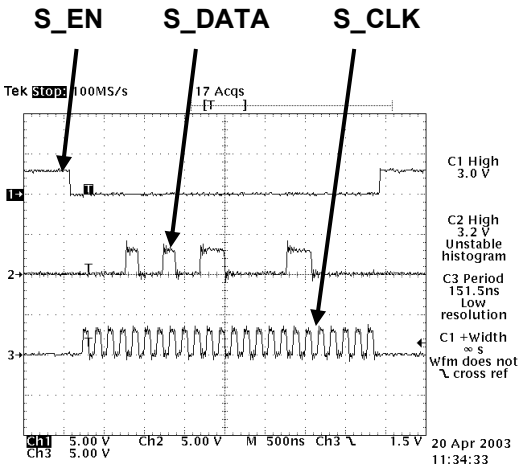


4.8.3 Checking PLL Circuit

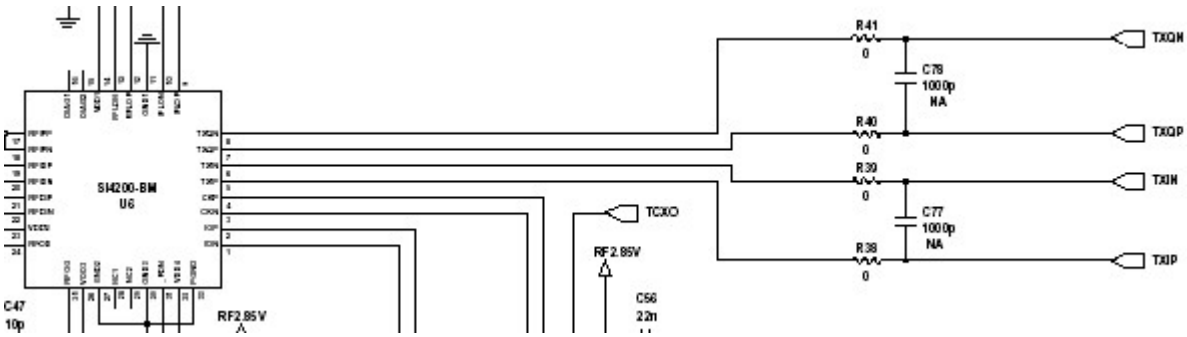


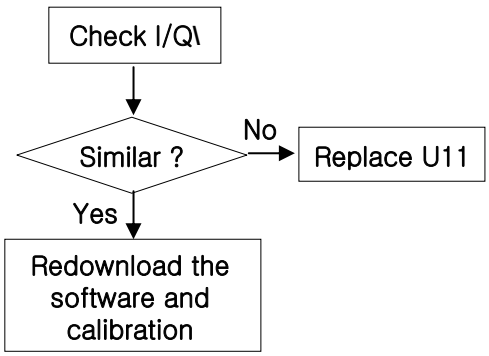


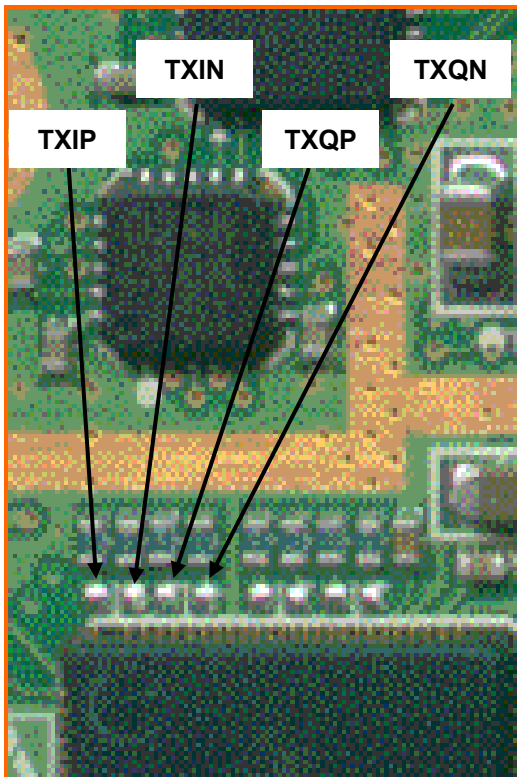


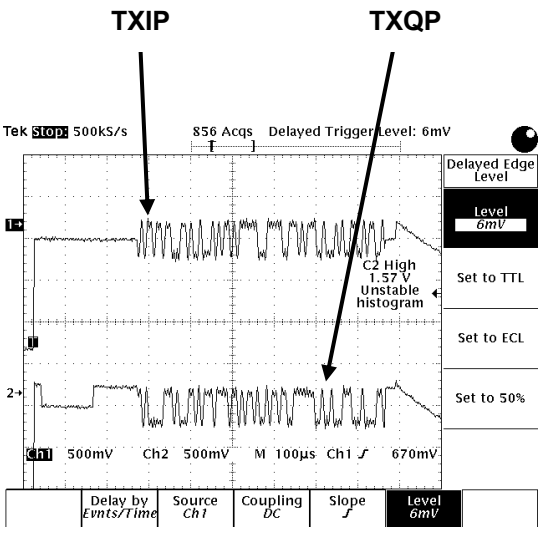


4.8.4 Checking TX I/Q

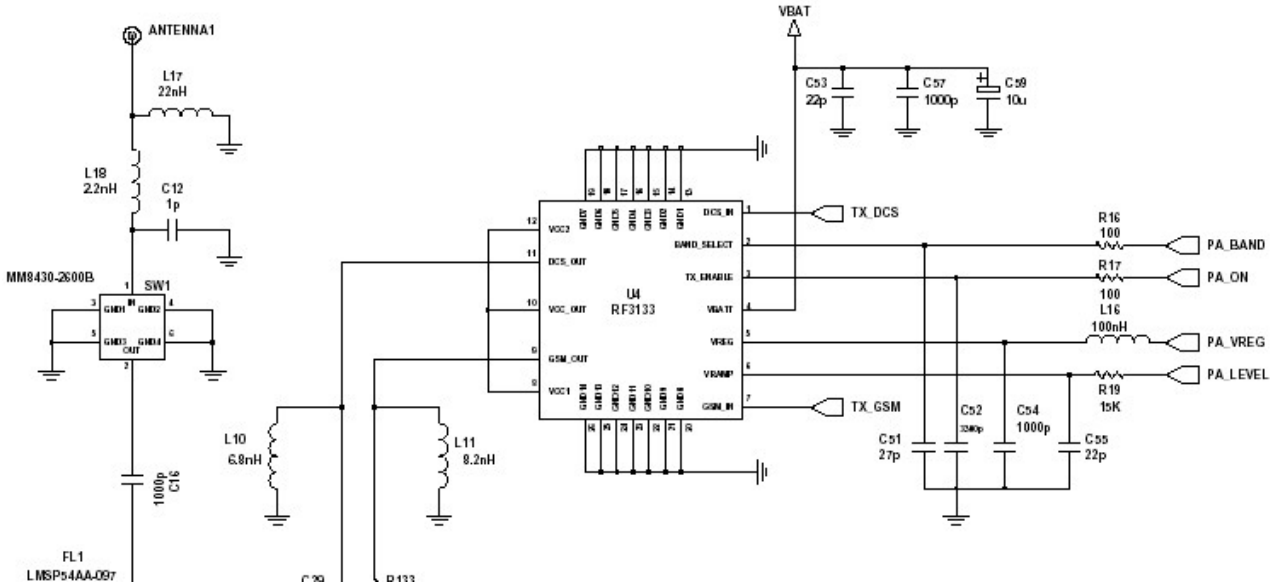


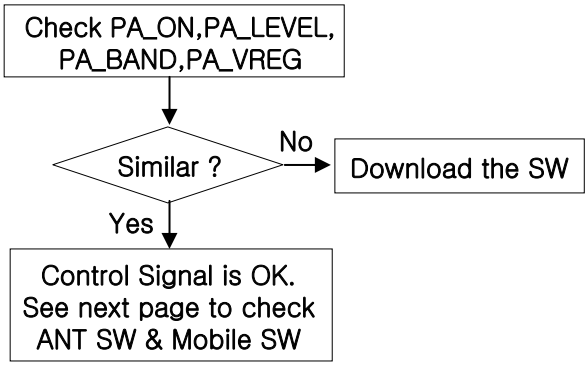


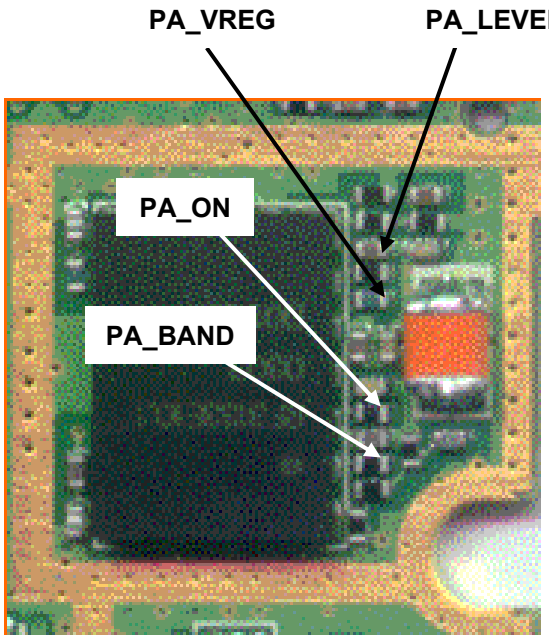


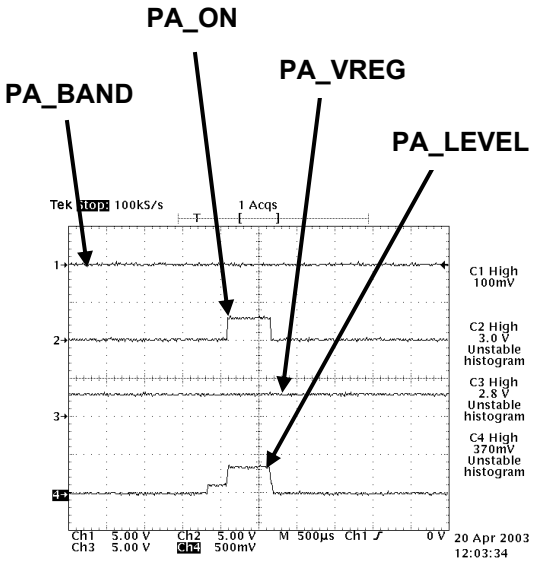


4.8.5 PAM Control Signal

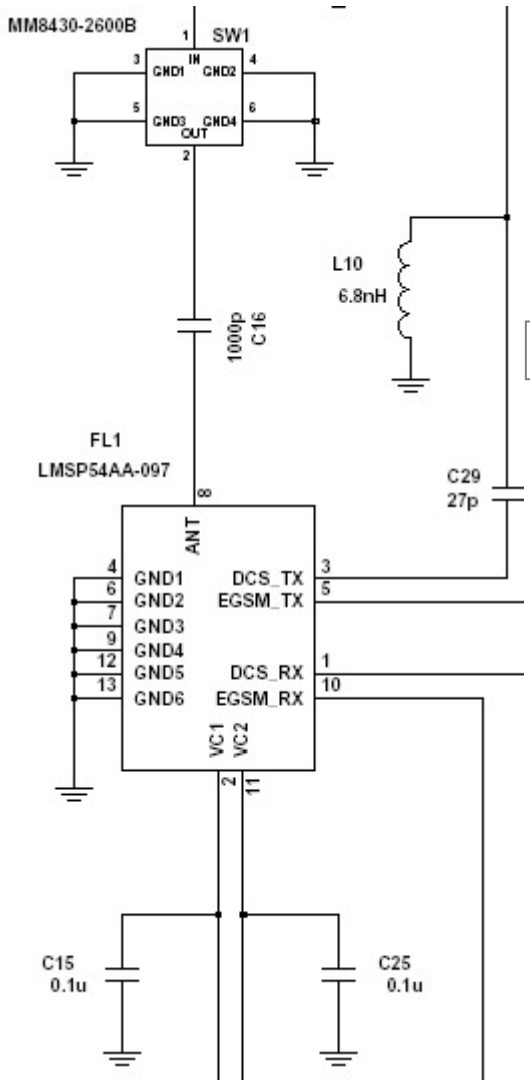


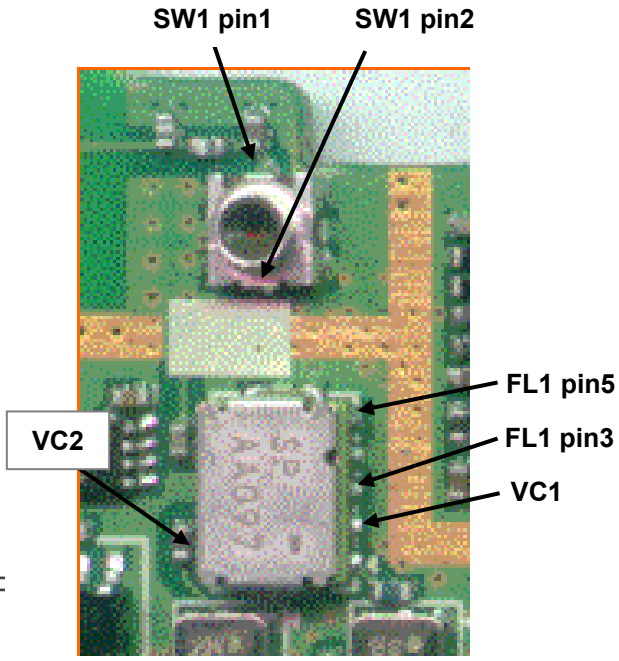


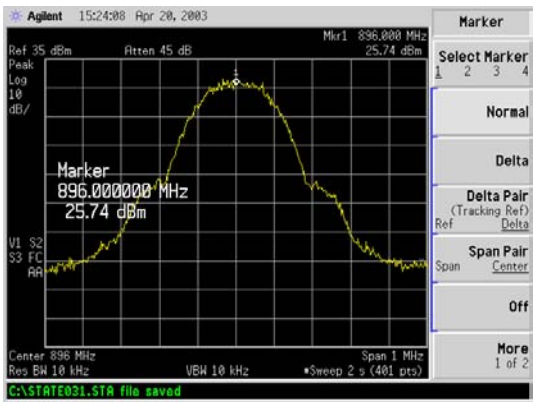


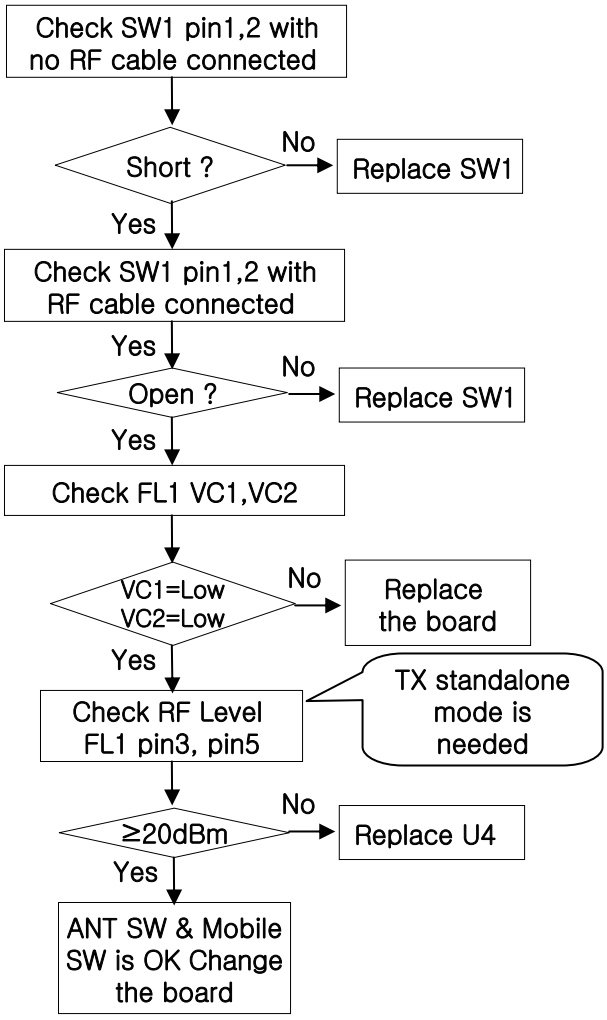


4.8.6 Checking ANT SW & Mobile SW









5. DOWNLOAD

A. Download Setup

Figure 5.1 describes Download Setup.

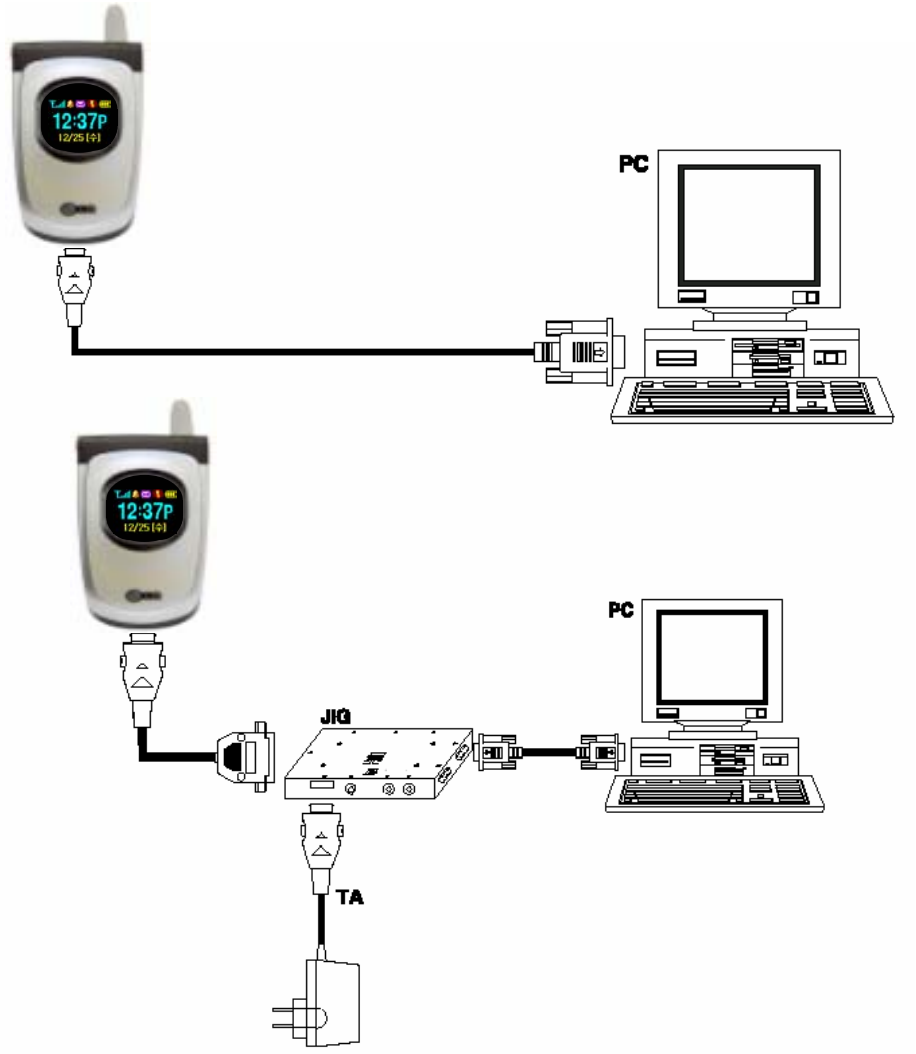
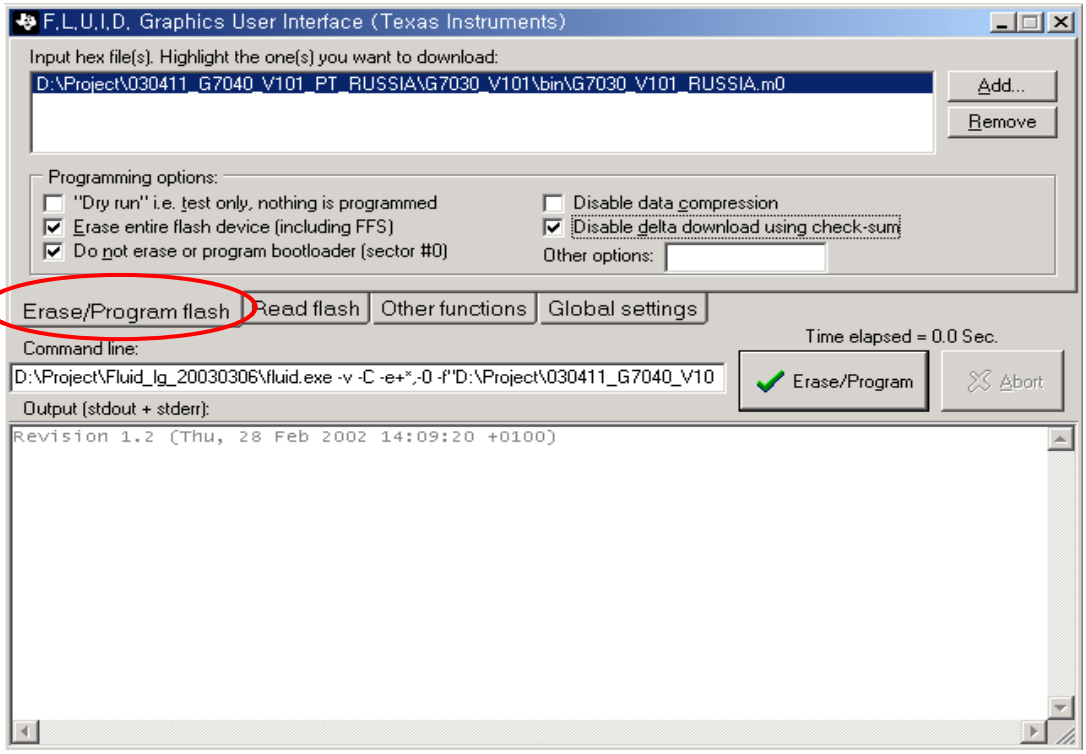


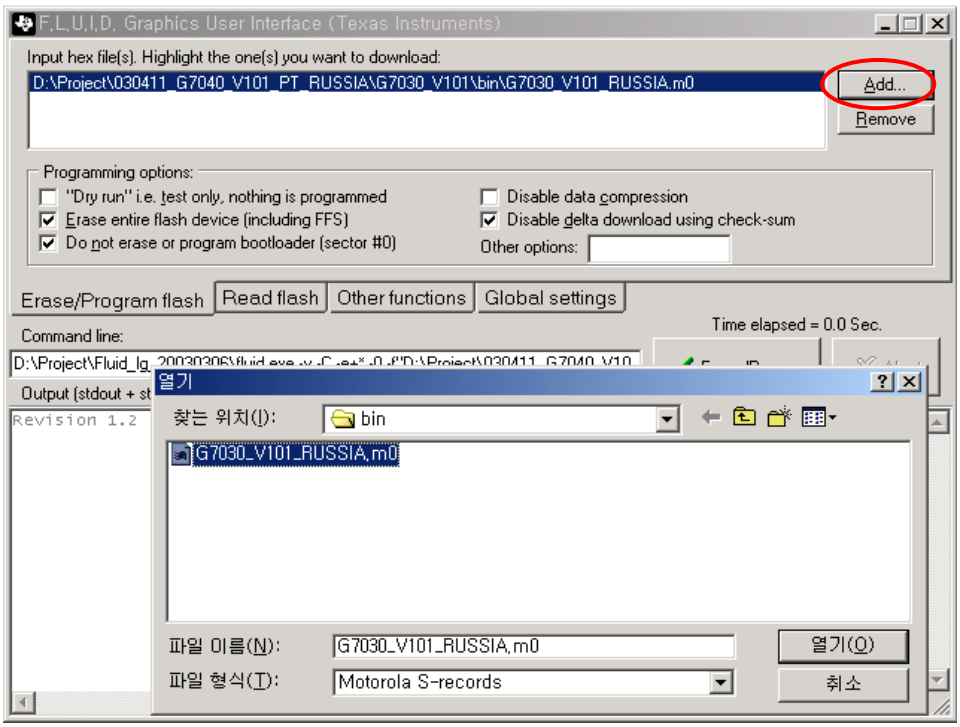
Figure 5.1 Download Setup

B. Download Procedure

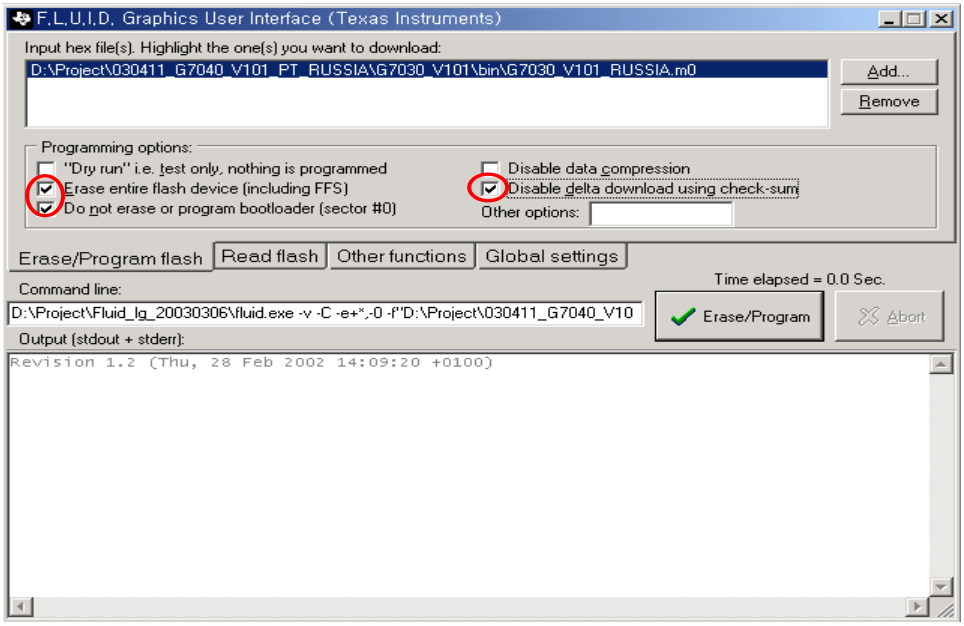
1. Execute Fluid_GUI.exe and select “Erase/Program flash” menu.



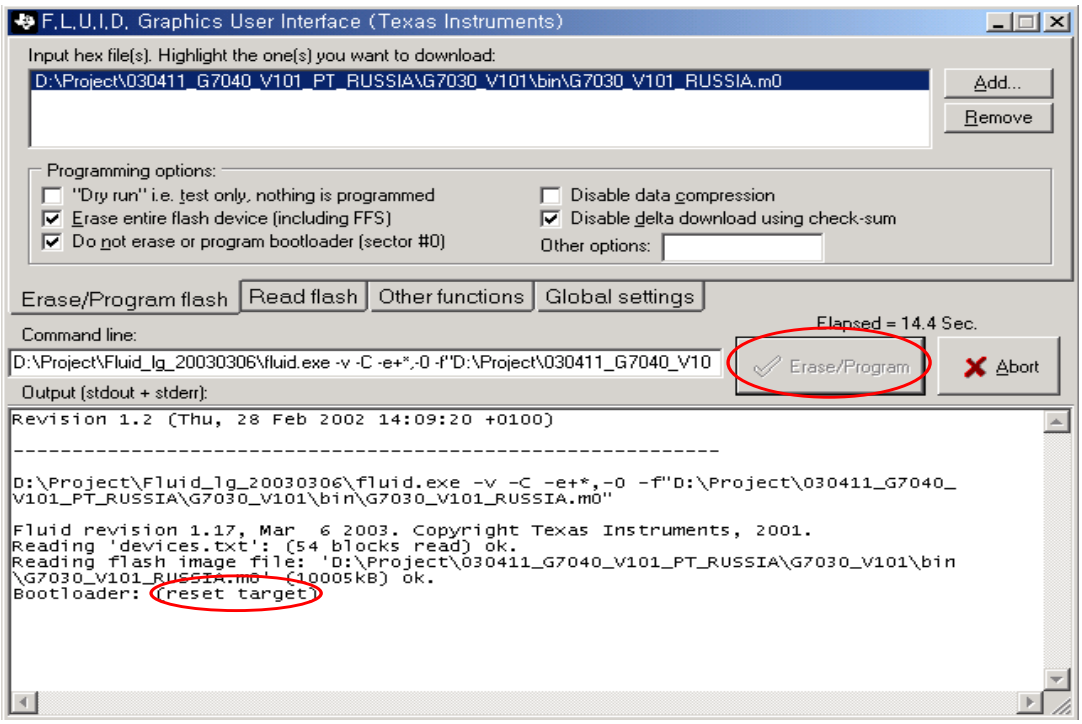
2. Click the “Add” button. Then, choose m0 file which is going to download.



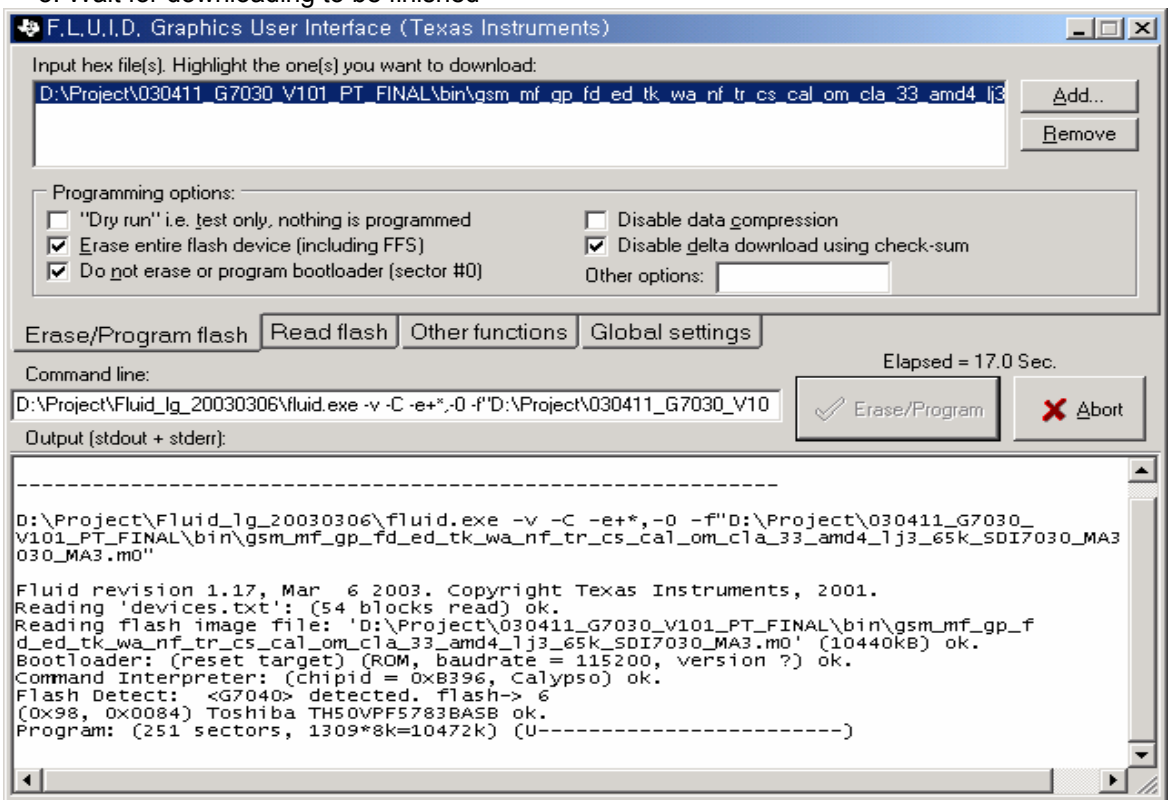
3. You must choose three programming options in programming options box. One is to decide whether you erase entire flash. If m0 file which is going to download have the change of pcm structure for current target's m0 file, you must erase entire flash memory. The second programming option is to decide whether you erase bootloader. It is recommended not to erase bootloader. The third is to decide whether you take delta-download, or not. If you use delta-download, You can save download time through comparing m0 and flash block, and not downloading flash block same with m0 file.



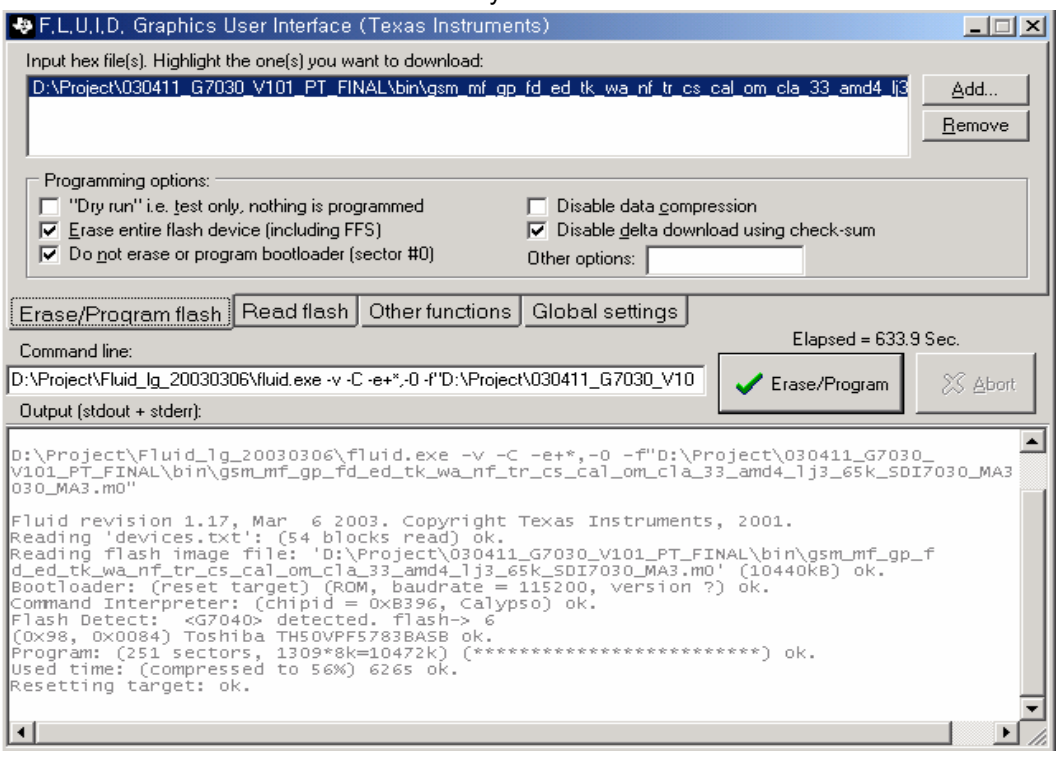
4. After checking programming options, Click "Erase/Program" button. If you click "Erase/Program" button, you will be able to see that "(reset target)" is displayed in the "Output" window. And then if you push shortly the "Power key" of the mobile, downloading will be started.



5. Wait for downloading to be finished



6. If downloading is finished, we can switch on the mobile. When you switch on the mobile first time after downloading, you must not remove the battery until switch-on procedure is completed. If you remove the battery before switch-on procedure is completed, we will not be able to save user data in the flash memory of the mobile



6. SERVICE S/W AND CALIBRATION

6.1. Service S/W

6.1.1 Overview

This service S/W is used for Calibration and Standalone test.

6.1.2 Hardware and Software Environment

• More than 486 computer
• 16Mbyte RAM
• Remained more than 10Mbyte in Hard Disk Memory
• Under Microsoft window 98 or more than

6.1.3 Software Installation

Unzip the phones service software provided where folder you want there are some files extracted in that folder. Start Setup.exe in Service software setup folder. RampTable.dat, default transmit ramping table, and rf_original_L300.epm, default calibration data, are located in window system folder so that these files are loaded automatically, if you execute LaputaService.exe.

6.1.4 Common Properties of Service Software

When you execute this program, you'll see the below user interface window titled *LAPUTA_Service Tool in* figure 6-1. The *LAPUTA_Service Too*l has five main frames.

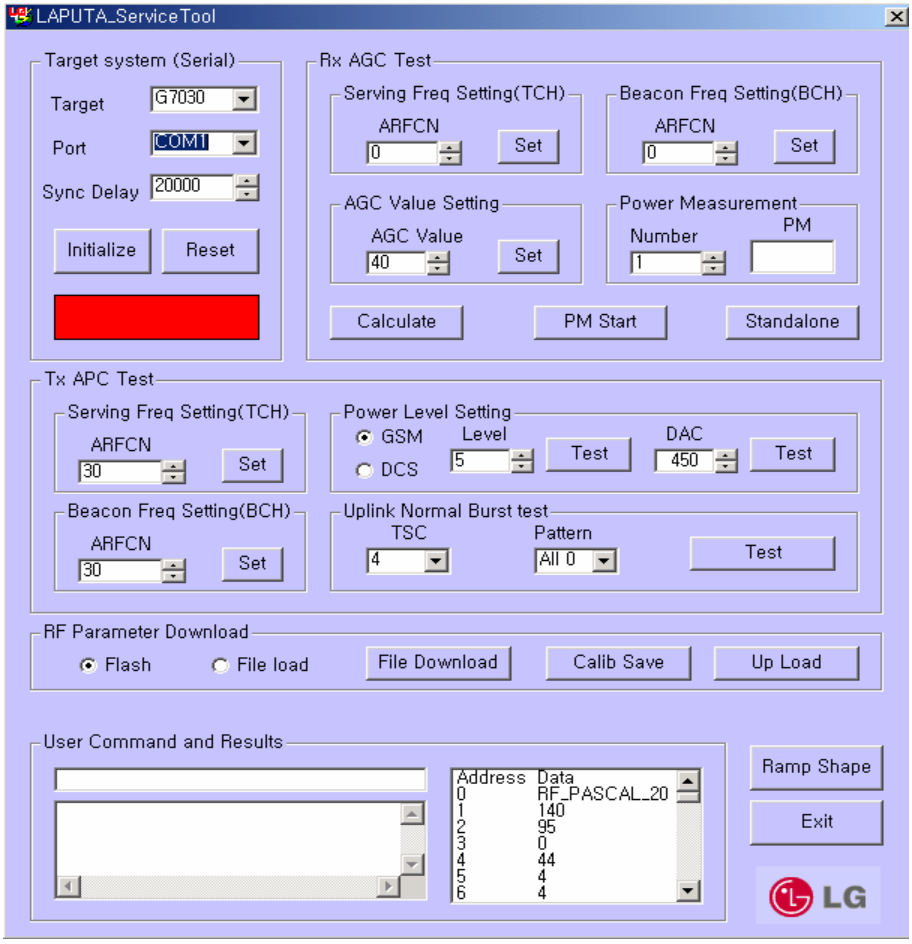


Figure 6-1. LAPUTA service tool

A. Target System Frame

This is for initializing the target phone. When you use this program to test G7000 phone, you have to initialize target at first. To initialize target phone, select target (G7000 is default) and COM port used at your computer and then click the Initialize button. If target initializing is ended successfully, the box in red below the initialize button will turn into green.

B. RX AGC Test Frame

At this part, you can control receiver path of target phone.

• **Serving Freq. Setting (TCH)**
You can set TCH of phone. The number means ARFCN of Traffic channel. You can change the value by clicking arrow button by one step or just entering the number directly.
• **Beacon Freq. Setting (BCH)**
You can set BCH of phone. The number means ARFCN of base station broadcasting channel.
• **AGC Value Setting**
You can set AGC gain of phone. The number means gain of AGC amplifier in Rx path.
• **Power Measurement**
The number means channel index according to pre-defined ARFCN. There are 12 pre-defined ARFCNs within Rx band. 4 ARFCNs are for GSM and others for DCS. Clicking arrow button to change number, you can see TCH and BCH ARFCN changed automatically. PM window displays the power level measured in baseband chip. PM value is useful to calculate the received absolute power. The unit of PM is dBd.
• **PM Start**
You can measure Rx power that target received from test equipment. When you click this button the result of power measurement displayed at PM blank in Power Measurement frame. You can measure PM for all 12-channel indexes by changing Number and clicking PM Start.
• **Calculate**
You have to do this work after measuring PM for all 12-channel indexes. When you click this button, service software calculate the calibration data from measured 12 PM data.
• **Standalone**
This button makes target operate in Rx mode continuously. Target will be operated under the condition that you set. During continuous receiving mode, label of Standalone button is changed to Stop. If you want stop receiving mode operating, click this button one more.

C. TX APC Test Frame

At this part, you can control transmit path of target phone.

• **Serving Freq. Setting (TCH)**
You can set TCH of phone. The number means ARFCN of Traffic channel.
• **Beacon Freq. Setting (BCH)**
You can set BCH of phone. The number means ARFCN of base station broadcasting channel.
• **Power Level Setting**
First, you have to choose operating mode (GSM or DCS) according to TCH and BCH frequency that you selected before. Then select the Level and adjust the DAC value. Level means GSM/DCS output power level. Usable range is 5 to 19 for GSM, 0 to 15 for DCS. DAC value is a factor to determine output power. Its variable range is 0 to 1023.
• **Uplink Normal Burst test**
You can also control the traffic slot number be using by changing TCS value. Because GSM has 8-time slot, TCS value varies 0 to 7. Patten is to select data format that is transmitted. You can send all data 0, or 1 or repeating of 1010. But it is good to you to using the default value because data format doesn't affect to RF characteristics.

Test
Transmitting is started when you click this button. During Transmitting, label of Test button is changed to Stop. If you want stop transmitting, click this button one more.

D. RF Parameter Download Frame

• **Saving epm file into Flash**
When you have a epm file, contains calibrated data, and you want to download into target Flash, check Flash and click File Download button. Then you can see RF parameters Save window. Select epm file you want to save into Flash then click Open. During saving file into Flash, The statement bar indicating download process is displayed under the RF Parameter Download frame. As successfully ending download, information box will be appeared. Click Ok.
• **Saving Cal. Data to Flash**
After Rx or Tx calibration, you can save the calibration results into Flash and epm file. Check Flash and click Calib Save button. Then you can see RF parameters Save window. Write the file name and click Save button.

E. User Command and Results Frame

Whenever you click button or make some event in service software, every ordered event is displayed in this frame. You can also see calibration results here.

F. Ramp shape button

This button is for burst shape table. But it is deactivated in service software.

6.2. Calibration

6.2.1 Overview

The calibration values of the phone reside on the Flash. The contents of the Flash can be read by the service software and saved as a file. This is advisable when there is need to retain that information, e.g. in view of replacement of the circuit. The program also enables writing the default parameters on the Flash, in which case all calibration steps should be carried out. The service software can't control the equipment, so only manual calibration process is possible.

6.2.2 Equipment List

Table 6-1. Calibration Equipment List.

Equipment for Calibration	Type / Model	Brand
Wireless Communication Test Set	HP 8960, HP8922, CMU200, any other call equipment	
RS-232 Cable and Test JIG		
RF Cable		
Power Supply		
Service SW	Laputa	
Test SIM card		
PC(For Software Installation)	Pentium II Class above 300MHz	

6.2.3 Equipment setup

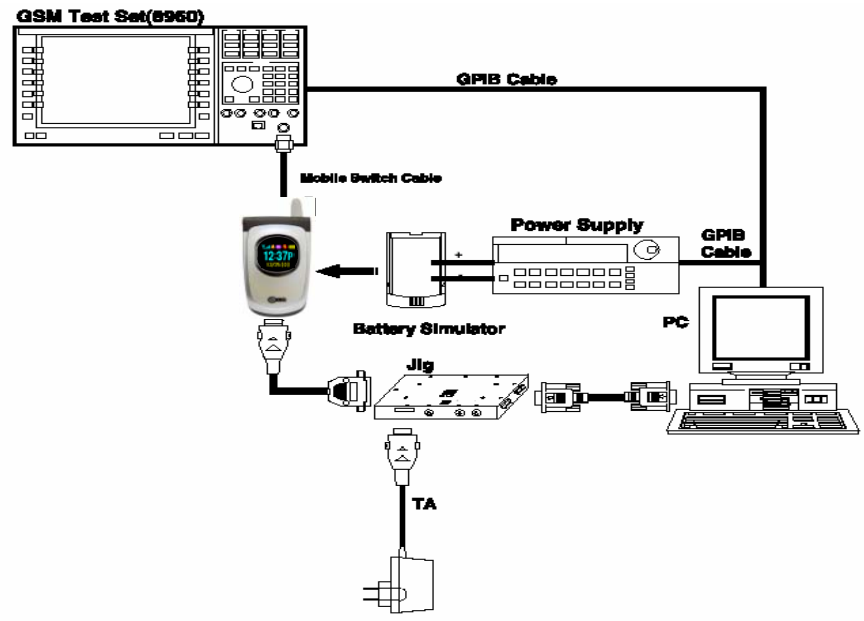


Figure 6-1. Calibration Equipment List..

6.2.4 Calibration steps

A. RX Calibration

In order for the RSSI measurements to be within the GSM specifications, some calibration is necessary. Also, due to AGC implementation, some AGC specific constants need calibration. In total, three calibrations are required per receive band, AGC calibration, channel compensation and temperature compensation. Of these, temperature compensation is not needed in replacement of the circuit. In AGC calibration the reference power fed into the phone via permanent antenna connector is –74dBm. In channel compensation, the channel numbers in Rx band are;

E-GSM band : 0, 40, 124, 975, and 1023.
DCS band : 512, 574, 636, 700, 760, 822 and 885.

Procedure

a) Initialize phone by clicking Initialize button.
b) Set the GSM test equipment CW mode and BCH and TCH of GSM test equipment '0', same with phone.
c) Set the power of GSM test equipment '–74dBm'.
d) Click the PM Start button, then the value, received power by phone, is displayed in PM measurement window at service software.
e) Change the BCH and TCH of phone by clicking the Number button and set the channel (BCH & TCH) of equipment to be same.
f) Click the PM Start button.
g) Repeat above procedure until the displayed number in Power Measurement window is 12.
h) Click the Calculate button, then the service software calculate the channel compensation parameters.
i) Saving updated calibration data into phone by clicking Calib Saving button.

NOTE

If the calibration does not done for all channels, 5 channels for EGSM900 and 7 channels for DCS1800, the service software reports, "Please execute after measuring the PM".

B. TX Calibration

In order for the Tx power to be within the GSM specifications for each Tx level, some calibration is necessary. In total, four calibrations are required per transmit band, power calibration, channel compensation, temperature compensation and low voltage compensation. Of these, temperature compensation and low voltage compensation are not needed in replacement of the circuit and channel compensation is not needed because the transmit power is in GSM specification with enough margin In power compensation, the channel numbers used in Tx band are;

E-GSM band : 62.
DCS band : 699.

And the target powers in dBm for each power level are;

Table 6-2. TX target Powers

Power level	GSM	DCS
0		29
1		28
2		26
3		24
4		22
5	32	20
6	31	18
7	29	16
8	27	14
9	25	12
10	23	10
11	21	8
12	19	6
13	17	4
14	15	2
15	13	0
16	11	
17	9	
18	7	
19	5	

Procedure

a) Initialize phone by clicking Initialize button.

b) Set the BCH and TCH of the phone 62 for E-GSM900 and 699 for DCS1800. Of cause you have to match test equipment's BCH and TCH ARFCN with this value. For each power level, adjust the DAC value to get target power and click Test button. Then you can see the output power displayed on test equipment.

c) Saving updated calibration data into phone by clicking Calib Saving button.

6.2.5 Test Jig Operation

JIG Power

	Description
Power Supply	Usually 4.0V
DC Adaptor	9.5V, 500mA

JIG DIP Switch

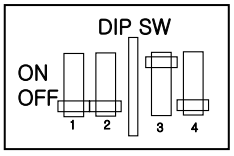
Switch Number	Name	Description
Switch1	ADI_REMOTE	In ON state phone is awaked. Not used set OFF state
Switch2	TI_REMOTE	In ON state phone is awaked
Switch3	VBAT	Power is provided for phone from power supply
Switch4	PS	Power is provided for phone form DC adaptor

JIG DIP Switch

LED Number	Name	Description
LED1	POWER	Power is provided for test jig
LED2	TA	Indicate charging state of the phone battery with travel charger
LED3	MON STATUS	Indicate date transfer state through the UART IRDA
LED4	UART STATUS	Indicate date transfer state through the UART MODEM

Operation

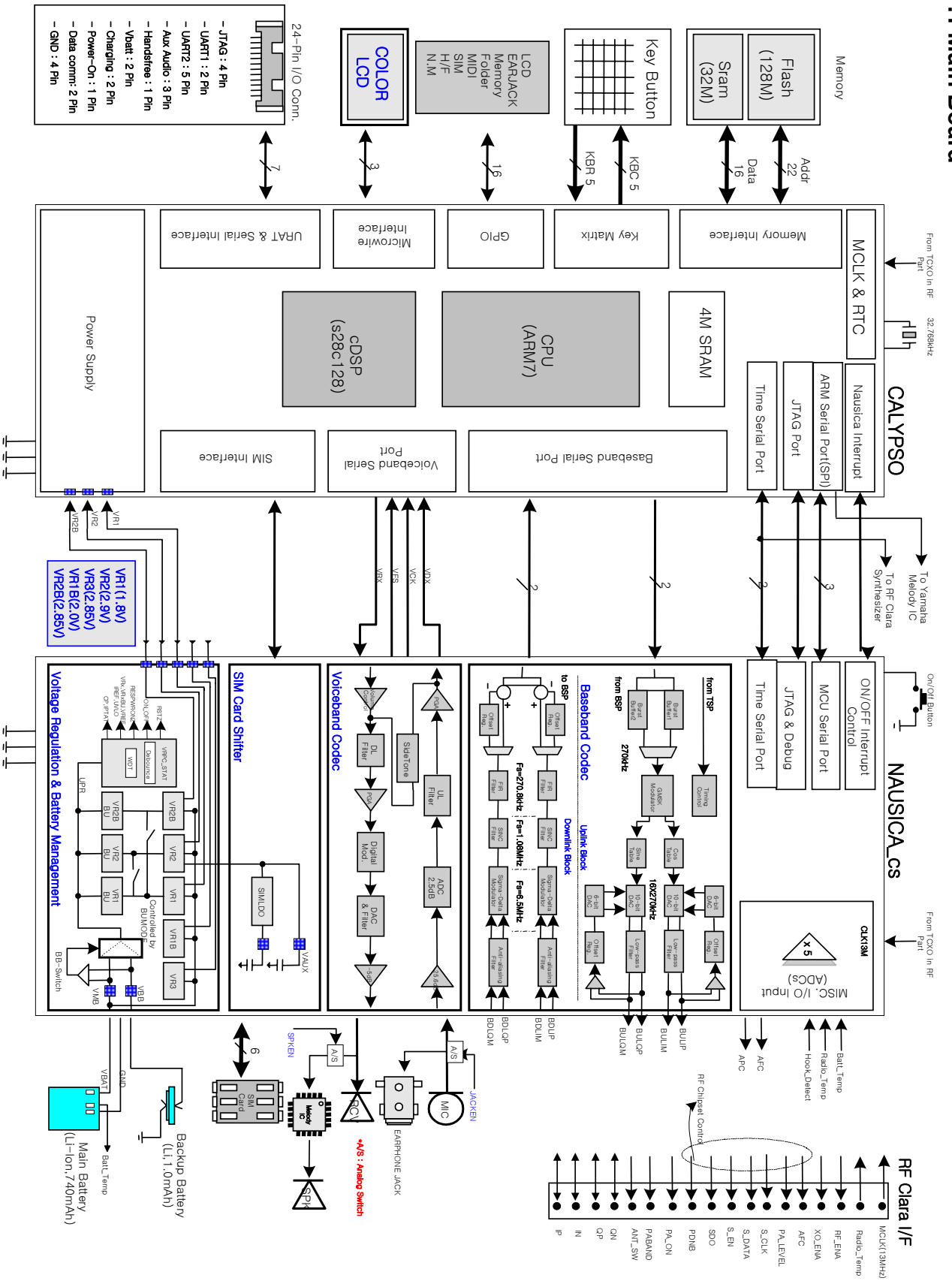
1) Connect the RS232 serial cable between COM port of notebook and MON port of test JIG in general
2) Set the power supply 4.0V
3) set the 3rd of DIP SW ON state.
4) set the 4th of DIP SW ON state.



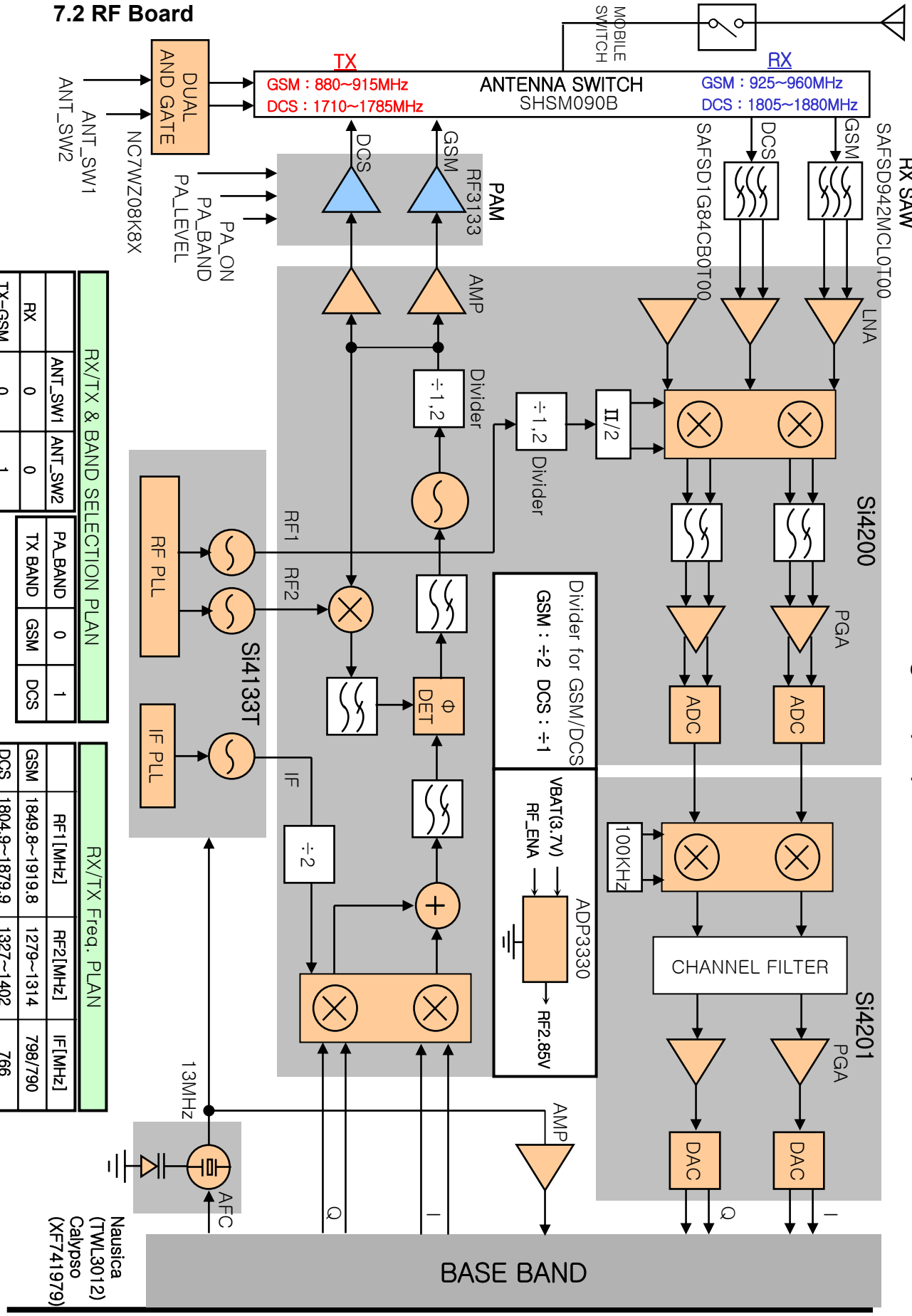
5) Press the phone power key. If the remote power on is used, switch the 1st of DIP SWITCH ON.

7. BLOCK DIAGRAM

7.1 Main Board



7.2 RF Board



	ANT_SW1	ANT_SW2
RX	0	0
TX-GSM	0	1
TX-DCS	1	0

RX/TX & BAND SELECTION PLAN

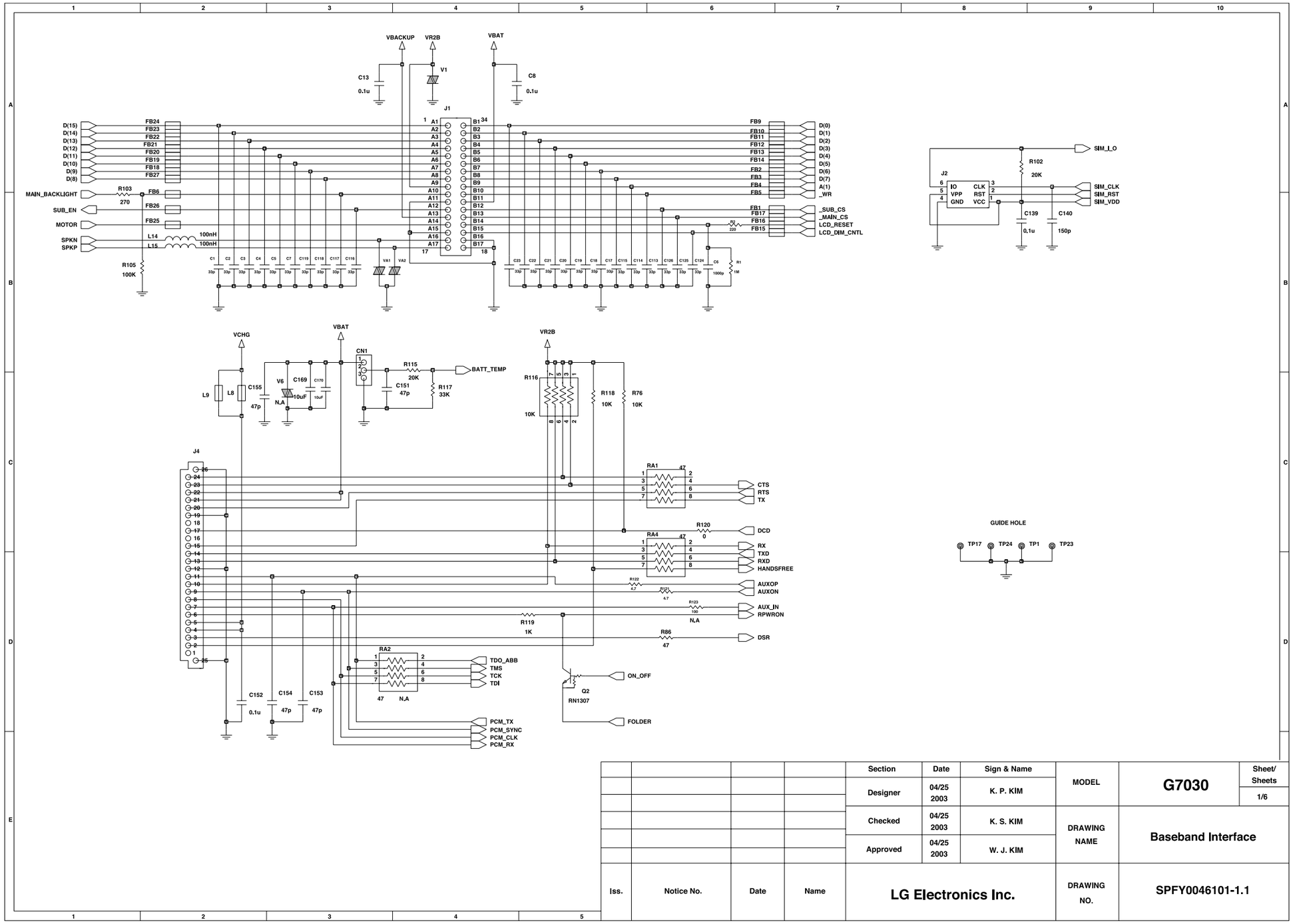
	PA_BAND
TX BAND	
GSM	0
DCS	1

	RF1[MHz]	RF2[MHz]	IF[MHz]
GSM	1849.8~1919.8	1279~1314	798/790
DCS	1804.9~1879.9	1327~1402	766

RX/TX Freq. PLAN

8. CIRCUIT DIAGRAM

8.1 Baseband Interface

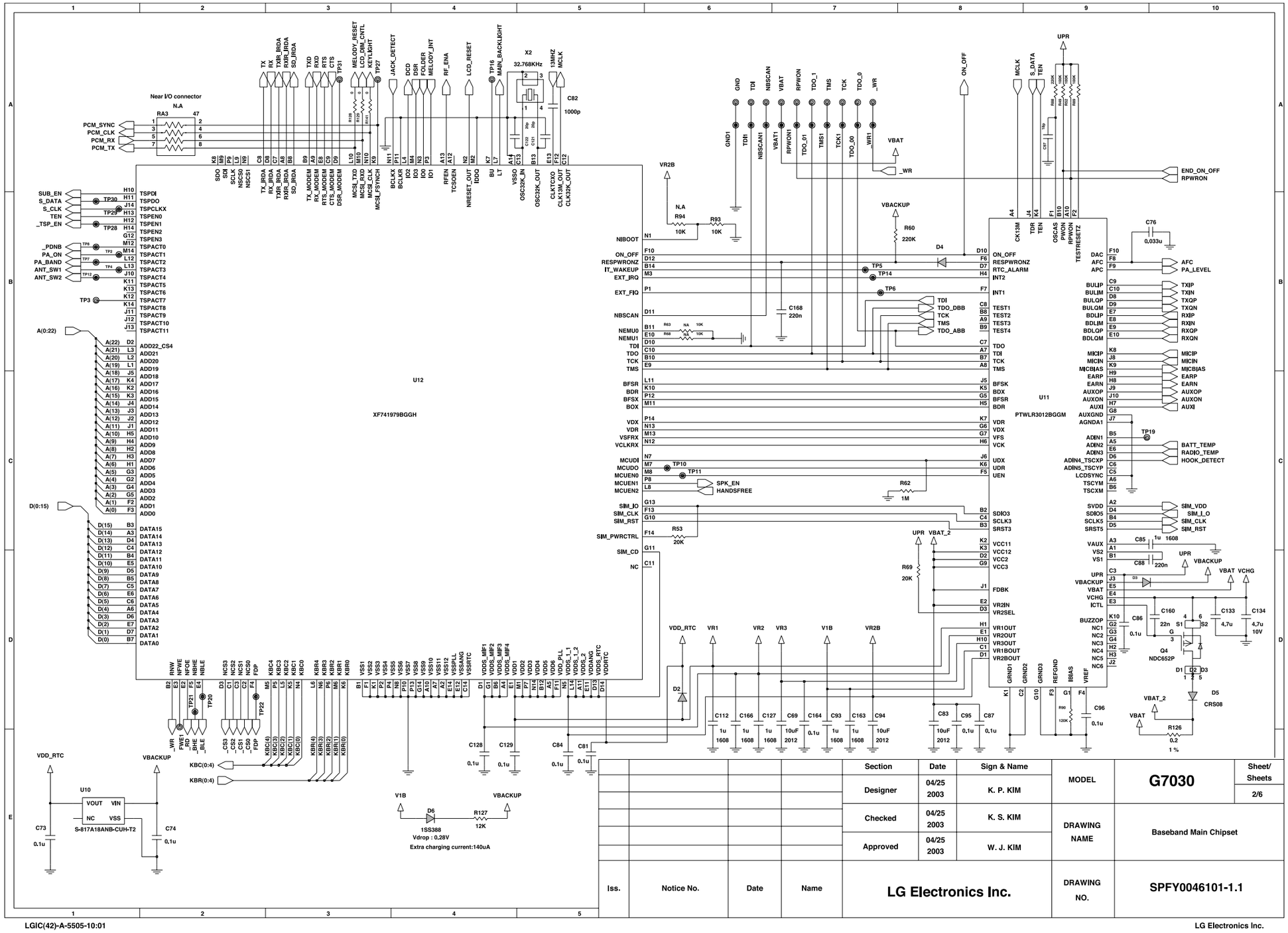


				Section	Date	Sign & Name	MODEL	G7030	Sheet/ Sheets
				Designer	04/25 2003	K. P. KIM			1/6
				Checked	04/25 2003	K. S. KIM	DRAWING NAME	Baseband Interface	
				Approved	04/25 2003	W. J. KIM			
Iss.	Notice No.	Date	Name	LG Electronics Inc.			DRAWING NO.	SPFY0046101-1.1	

LGIC(42)-A-5505-10:01

LG Electronics Inc.

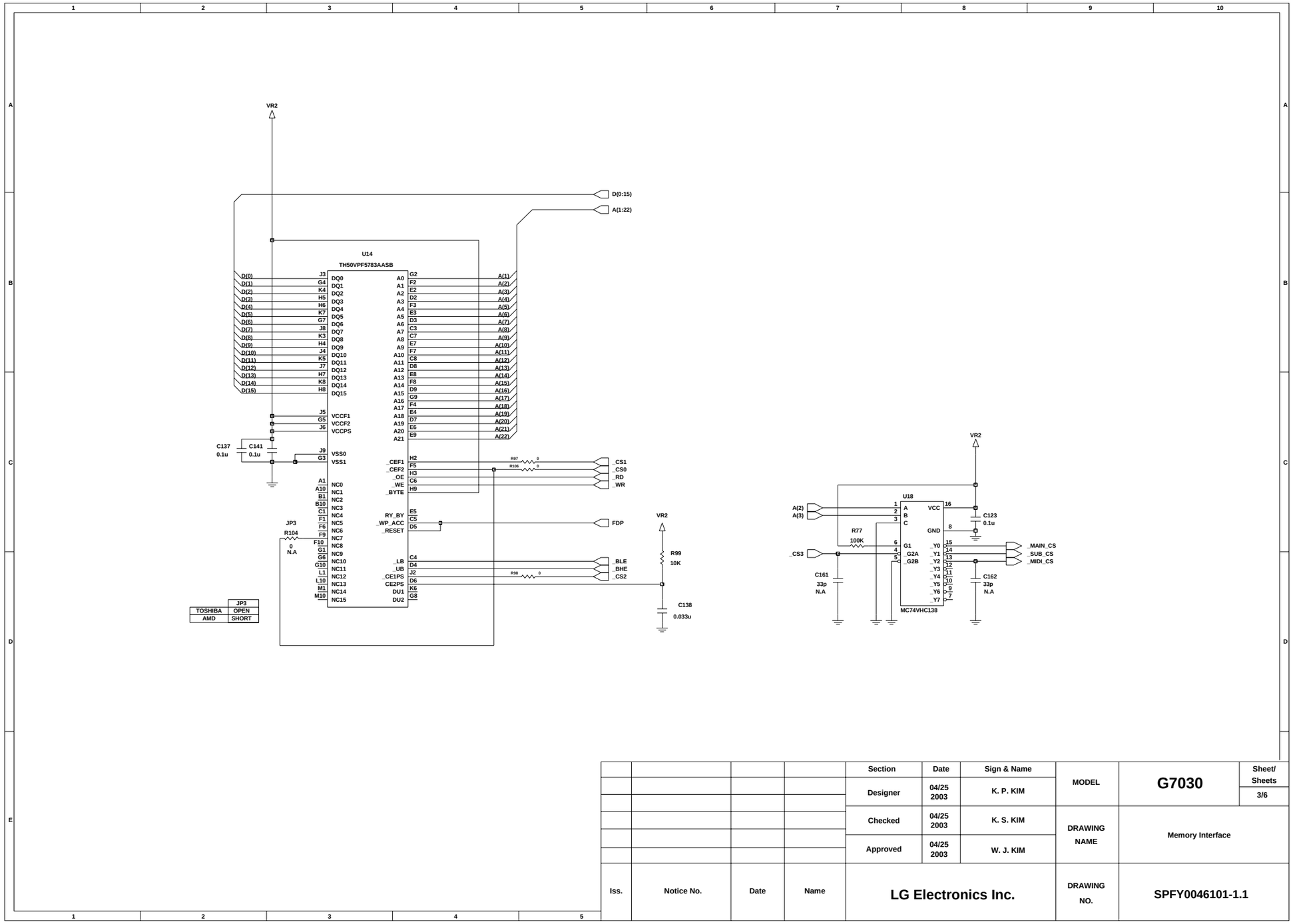
8.2 Baseband Main Chipset



LGIC(42)-A-5505-10:01

LG Electronics Inc.

8.3 Memory Interface

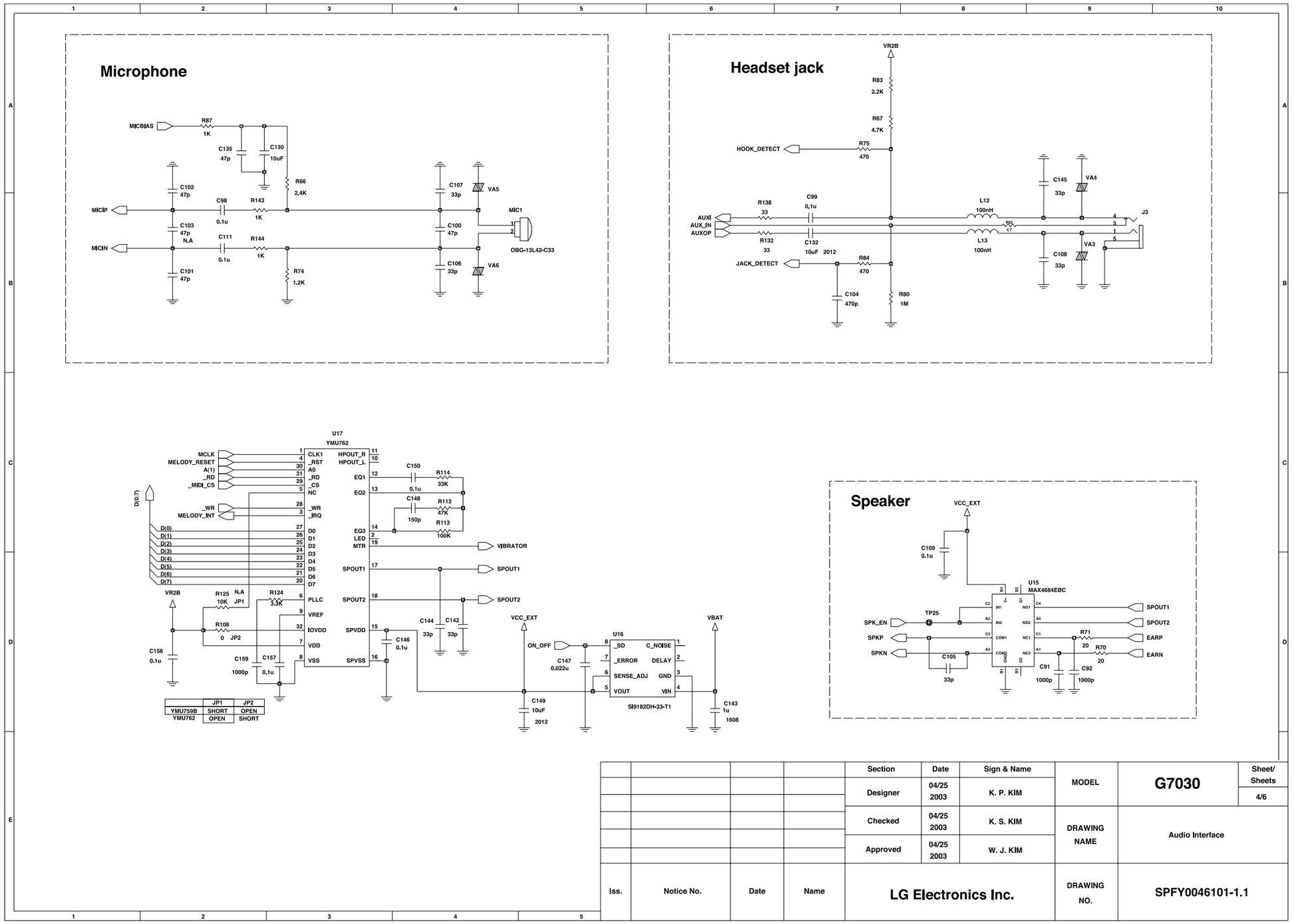


				Section	Date	Sign & Name	MODEL	G7030	Sheet/ Sheets
				Designer	04/25 2003	K. P. KIM			3/6
				Checked	04/25 2003	K. S. KIM	DRAWING NAME	Memory Interface	
				Approved	04/25 2003	W. J. KIM			
Iss.	Notice No.	Date	Name	LG Electronics Inc.			DRAWING NO.	SPFY0046101-1.1	

LGIC(42)-A-5505-10:01

LG Electronics Inc.

8.4 Audio Interface

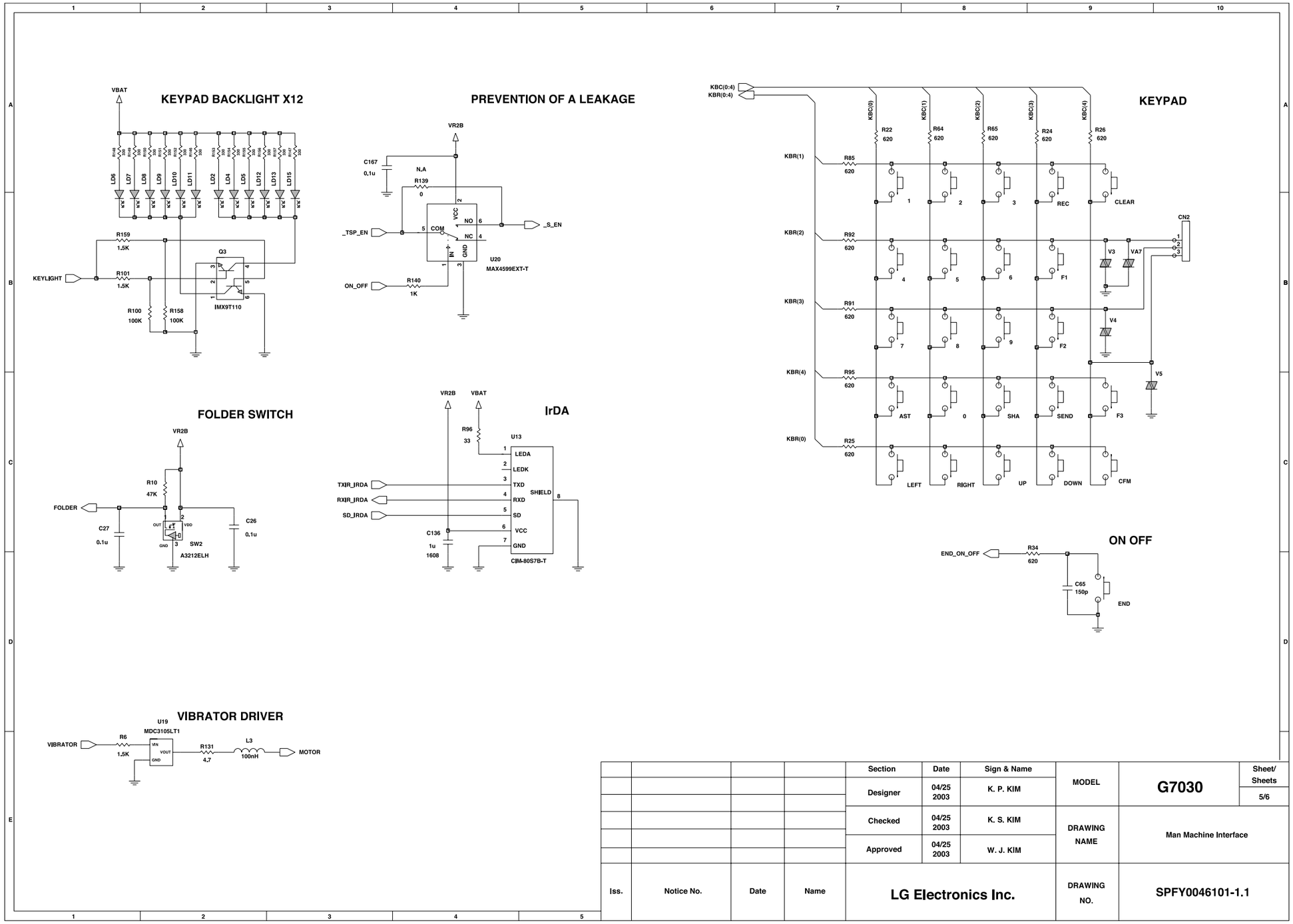


				Section	Date	Sign & Name	MODEL	G7030	Sheet/ Sheets
				Designer	04/25 2003	K. P. KIM			4/6
				Checked	04/25 2003	K. S. KIM	DRAWING NAME	Audio Interface	
				Approved	04/25 2003	W. J. KIM			
Iss.	Notice No.	Date	Name	LG Electronics Inc.			DRAWING NO.	SPFY0046101-1.1	

LGIC(42)-A-5505-10:01

LG Electronics Inc.

8.5 Man Machine Interface

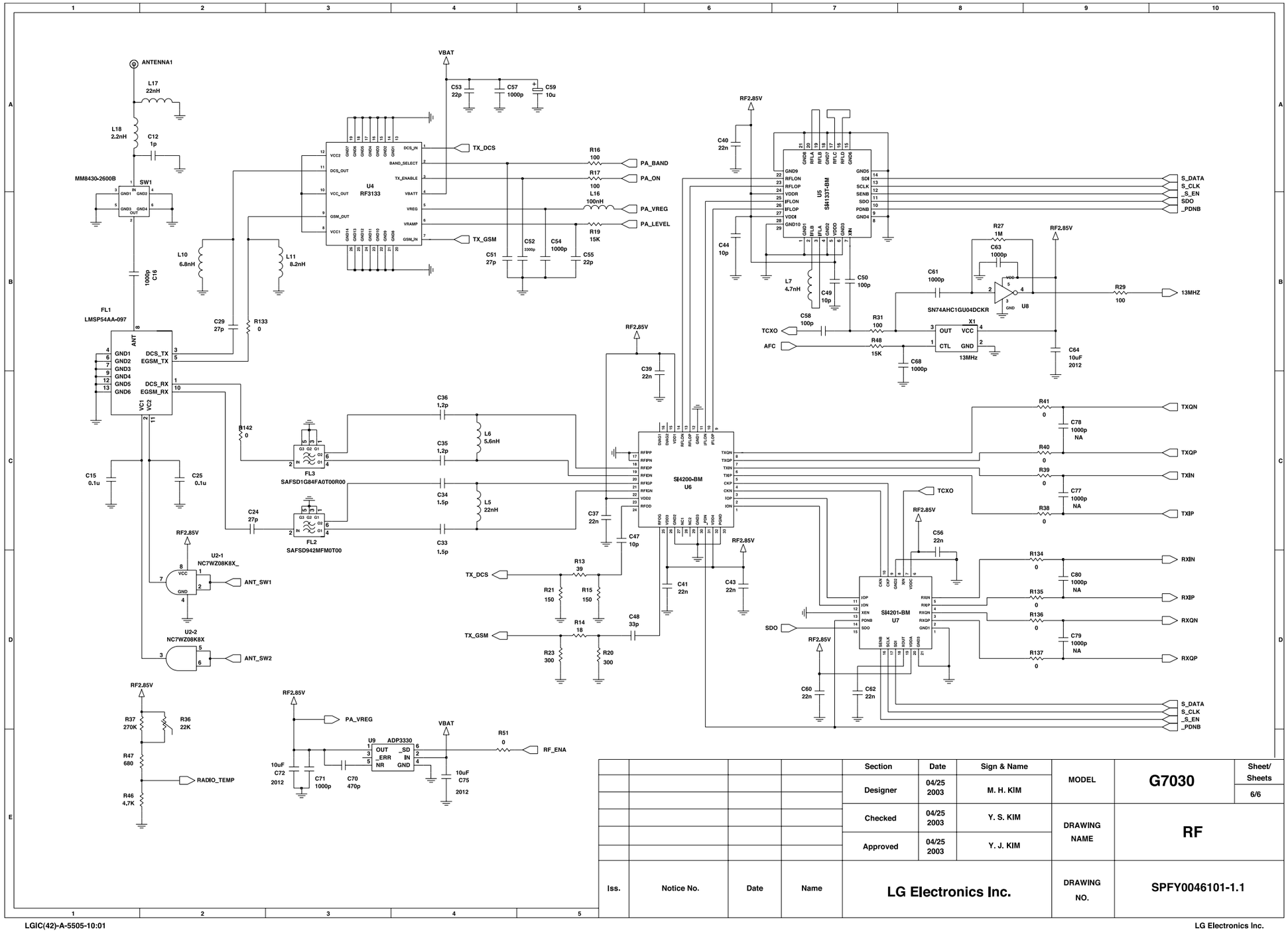


				Section	Date	Sign & Name	MODEL	G7030	Sheet/ Sheets
				Designer	04/25 2003	K. P. KIM			5/6
				Checked	04/25 2003	K. S. KIM	DRAWING NAME	Man Machine Interface	
				Approved	04/25 2003	W. J. KIM			
Iss.	Notice No.	Date	Name	LG Electronics Inc.			DRAWING NO.	SPFY0046101-1.1	

LGIC(42)-A-5505-10:01

LG Electronics Inc.

8.6 RF Interface



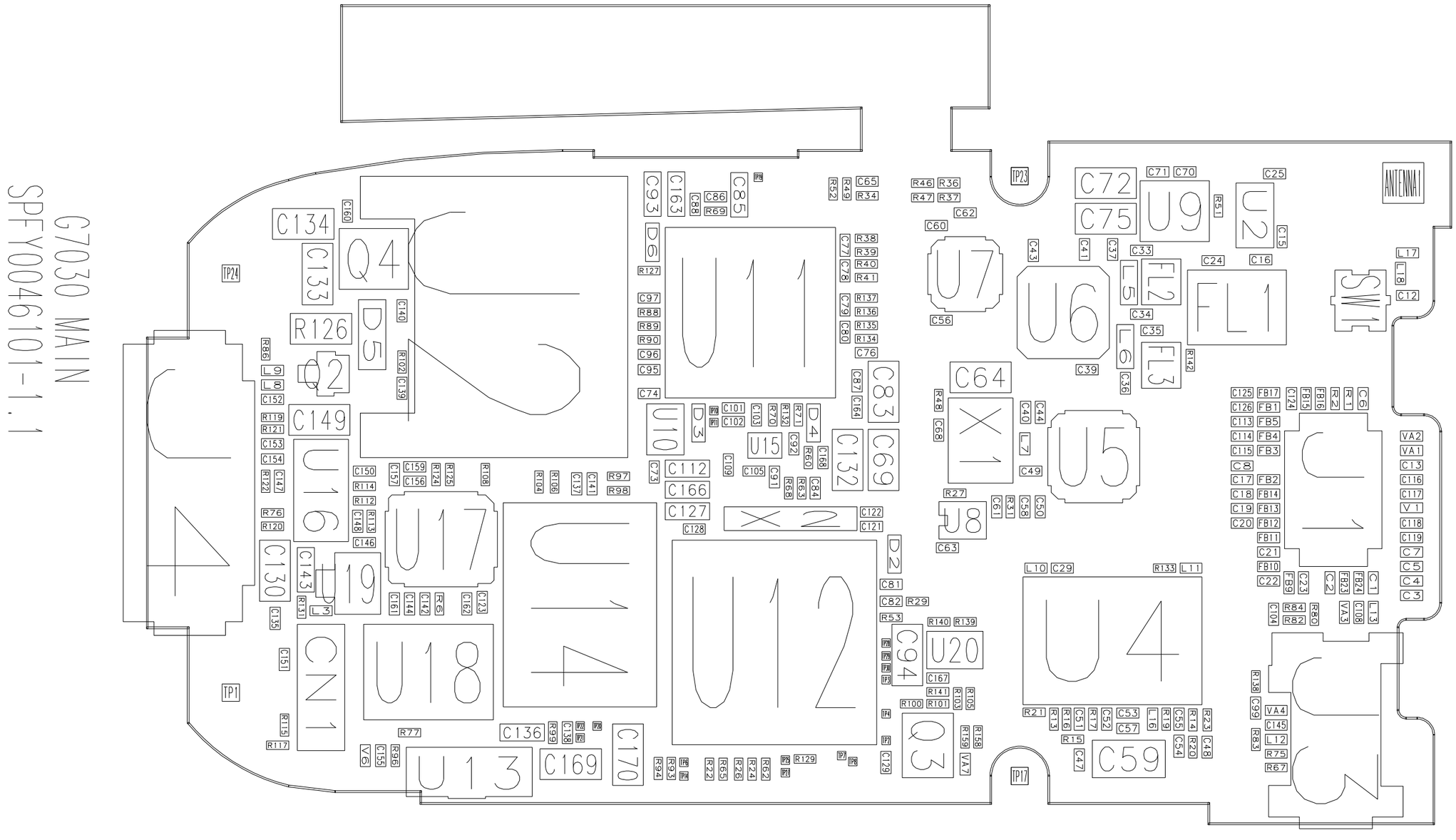
				Section	Date	Sign & Name	MODEL	G7030	Sheet/ Sheets
				Designer	04/25 2003	M. H. KIM			6/6
				Checked	04/25 2003	Y. S. KIM	DRAWING NAME	RF	
				Approved	04/25 2003	Y. J. KIM			
Iss.	Notice No.	Date	Name	LG Electronics Inc.			DRAWING NO.	SPFY0046101-1.1	

LGIC(42)-A-5505-10:01

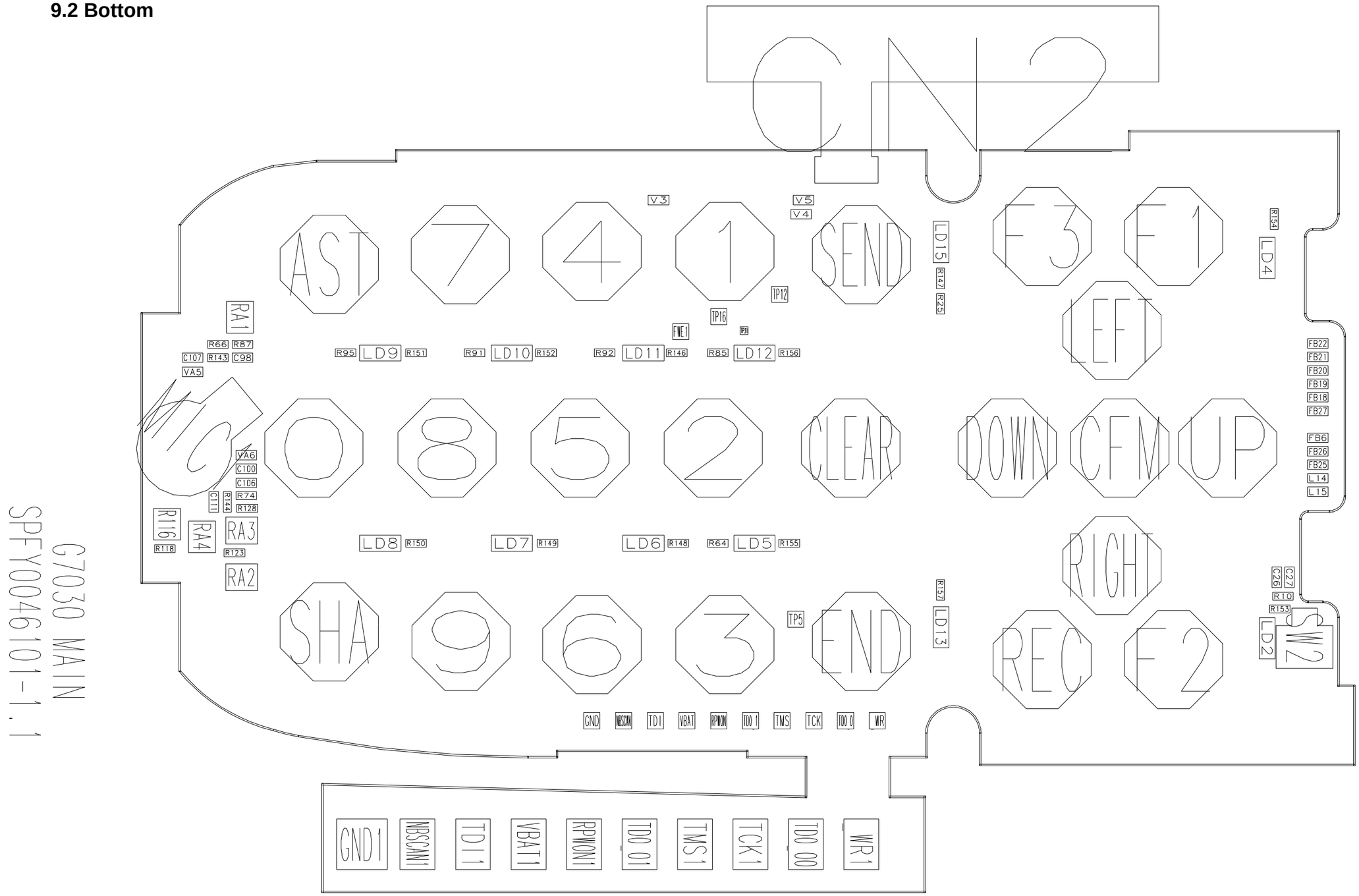
LG Electronics Inc.

9. PCB LAYOUT

9.1 Top



9.2 Bottom


C702
AST
7
4
1
SEND
F3
F1
EF
0
8
5
2
CLEAR
DOWN
CFM
UP
SHA
9
6
3
END
RIGH
REC
F2
G7030 MAIN
SPFY0046101-1.1

10. ENGINEERING MODE

Engineering mode is designed to allow a service man/engineer to view and test the basic functions provided by a handset. The key sequence for switching the engineering mode on is “2945#*# “Select. Pressing END will switch back to non-engineering mode operation. Use Up and Down key to select a menu and press ‘select’ key to progress the test. Pressing ‘back key will switch back to the original test menu.

[1] All auto test

[2] Baseband test

- [2-1] LCD
  - [2-1-1] LCD AUTO
  - [2-1-2] LCD CONTRAST
  - [2-1-3] 65K LCD TEST
- [2-2] FONT
  - [2-2-1] FONT 8 X 10
  - [2-2-2] FONT 8 X 10 I
  - [2-2-3] FONT 8 X 16
  - [2-2-4] FONT 8 X 16 I
  - [2-2-5] FONT 8 X 16 B
  - [2-2-6] FONT 10 X 19
  - [2-2-7] FONT 13 X 20
  - [2-2-8] FONT CHINA
- [2-3] ALERT
  - [2-3-1] VIBRATOR
  - [2-3-2] RING
  - [2-3-3] EFFECT SOUND
  - [2-3-4] IMELODY TEST
  - [2-3-5] EMS SOUND
  - [2-3-6] VOLUME
- [2-4] SERIAL PORT
  - [2-4-1] MODEM
  - [2-4-2] IrDA
- [2-5] BATTERY INFO1
- [2-6] AUDIO GAIN
  - [2-6-1] RECEIVER
  - [2-6-2] EAR MIC
  - [2-6-3] LOUD SPEAKER
  - [2-6-4] HANDSFREE
  - [2-6-5] DEFAULT VALUE

[3] S/W VERS

[4] ENG MODE

- [4-1] SYSTEM CHECK
- [4-2] CELL ENVIRON
- [4-3] LOCATION INFO
- [4-4] LAYER1 INFO
- [4-5] SYSTEM INFO1
- [4-6] SYSTEM INFO2
- [4-7] SYSTEM INFO3
- [4-8] SYSTEM INFO4
- [4-9] SYSTEM INFO5
- [4-0] SYSTEM INFO6
- [4-*] SYSTEM INFO78
- [4-#] SYSTEM INFO13

[5] FACTORY DEFAULT

11. STAND ALONE TEST

11.1 Setting Method

11.1.1 COM port

In the “Dialog Menu”, select the values as explained below.

- Port : select a correct COM port
- Baudrate : 38400
- Leave the rest as default values

11.1.2 Tx Test

1. Selecting Channel

- Select one of GSM or DCS Band and input appropriate channel.

2. Selecting APC

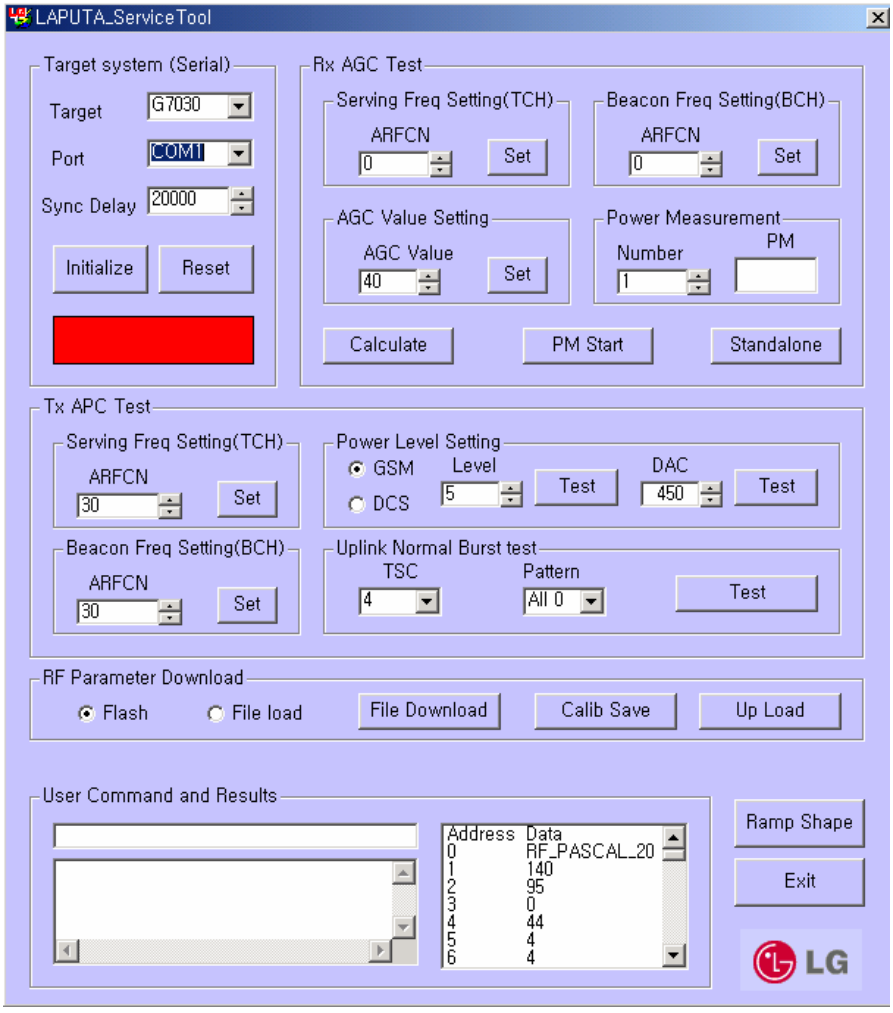
a. Select either Power level or DAC value.

b. Power level

- Input appropriate value GSM (between 5~19) or DCS (between 0~15)

c. DAC value

- You may adjust directly the power level with DAC values.



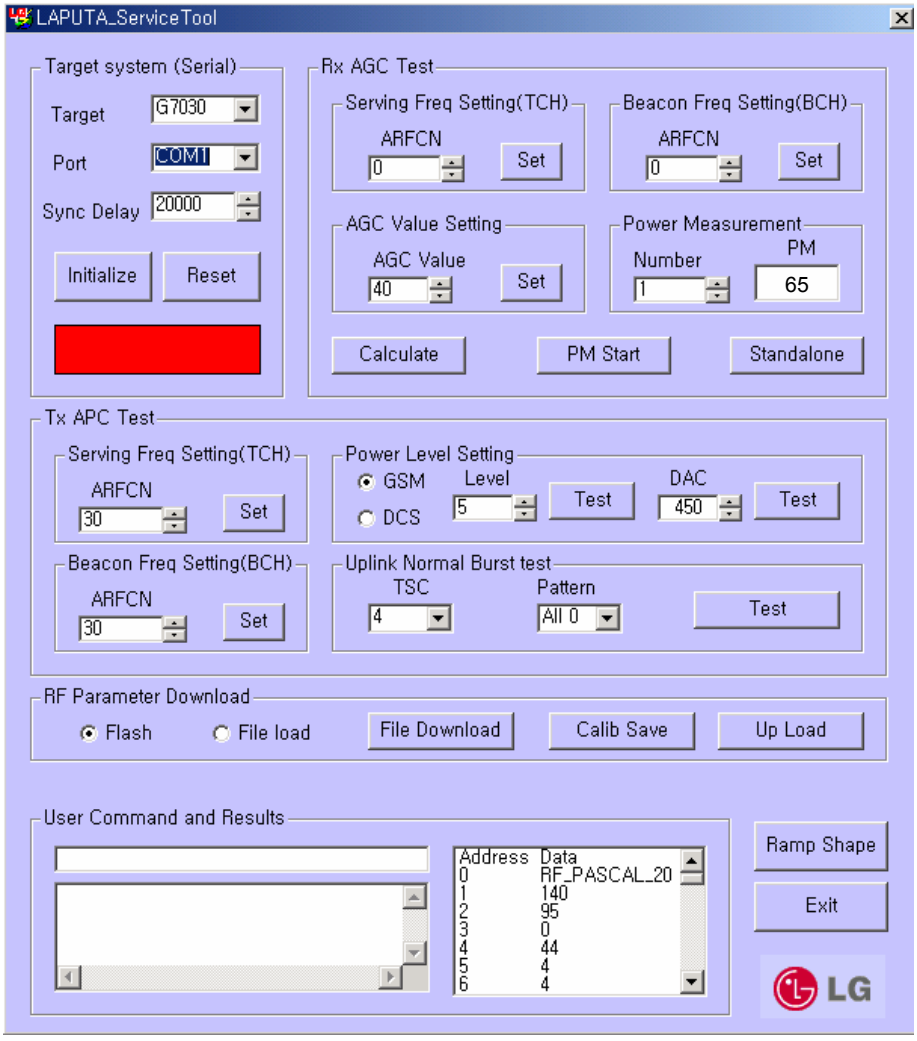
11.1.3 Rx Test

1. Selecting Channel

- Select one of GSM or DCS Band and input appropriate channel.

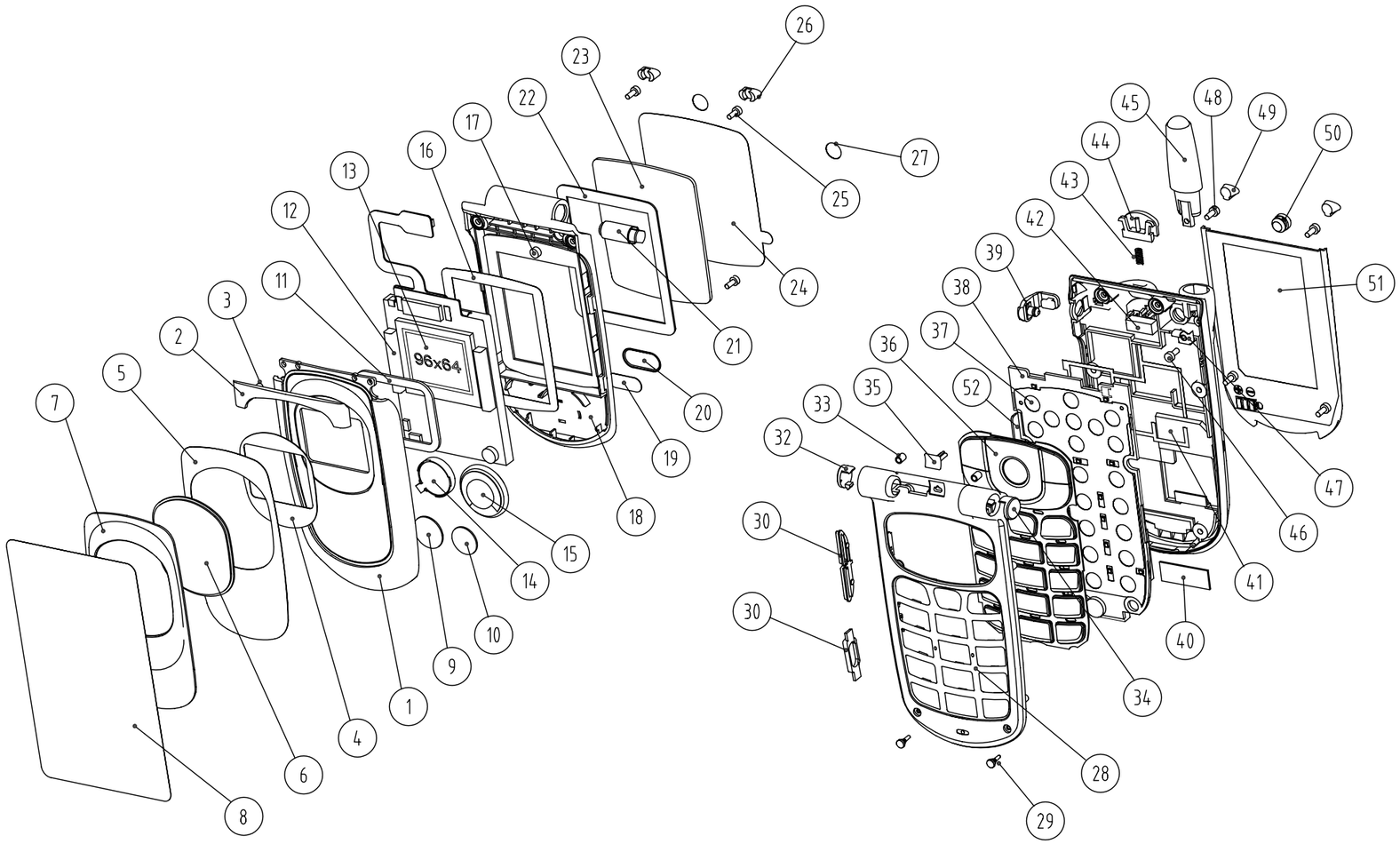
2. Automatic Gain Control and Instrument Power level

- See if the value of RSSI is close to -60dBm when setting the value 40 AGC Value Setting.
- Normal phone should indicate the value of RSSI close to -60dBm.



12. EXPLODED VIEW & REPLACEMENT PART LIST

12.1 Exploded View



No.	PART NAME	Q'TY	TYPE
52	PCB ASSY,SIDE KEY	1	ASSEMBLY
51	BATTERY PACK,LI-ION	1	ASSEMBLY
50	CAP,MOBILE SWITCH	1	PART
49	CAP,SCREW(REAR)	2	PART
48	SCREW,MACHINE(M1.4x3.5)	6	PART
47	CONTACT,ANTENNA	1	PART
46	SCREW,MACHINE(M1.4x3.5)	1	PART
45	ANTENNA,GSM,FIXED	1	PART
44	LOCKER,BATTERY	1	PART
43	SPRING,COIL	1	PART
42	GASKET,SHIELD FOAM(FPCB)	1	PART
41	COVER,REAR	1	PART
40	GASKET,SHIELD FOAM(IO CN)	1	PART
39	CAP,EARPHONE JACK	1	PART
38	PCB ASSY,MAIN	1	ASSEMBLY
37	DOME ASSY,METAL	1	PART
36	BUTTON ASSY,DIAL	1	ASSEMBLY
35	STOPPER,HINGE	1	PART
34	INSERT(M1.4xL2.5)	6	PART
33	DECO,HINGE(RIGHT)	1	PART
32	DECO,HINGE(LEFT)	1	PART
31	BUTTON ASSY,SIDE	1	PART
30	WINDOW,IRDA	1	PART
29	BUMPER	2	PART
28	COVER,FRONT	1	PART
27	CAP,SCREW(FOLDER)_Sheet	2	PART
26	CAP,SCREW(FOLDER)_Rubber	2	PART
25	SCREW,MACHINE(M1.4x3.5)	3	PART
24	TAPE,PROTECTION(WINDOW)	1	PART
23	WINDOW,LCD	1	PART
22	TAPE,WINDOW	1	PART
21	HINGE,FOLDER(5.8D)	1	PART
20	DECO,RECEIVER	1	PART
19	TAPE,DECO(RECEIVER)	1	PART
18	COVER,FOLDER(LOWER)	1	PART
17	MAGNET,SWITCH	1	PART
16	PAD,LCD	1	PART
15	SPEAKER	1	PART
14	VIBRATOR,MOTOR	1	PART
13	LCD MODULE ASSY	1	ASSEMBLY
12	GASKET,SHIELD FORM(LCD)	2	PART
11	PAD,LCD(SUB)	1	PART
10	PAD,RECEIVER	1	PART
9	PAD,MOTOR	1	PART
8	TAPE,PROTECTION(UPPER)	1	PART
7	DECO,WINDOW(SUB)	1	PART
6	WINDOW,LCD(SUB)	1	PART
5	TAPE,DECO(AL)	1	PART
4	TAPE,WINDOW(SUB)	1	PART
3	INSERT(M1.4xL2.5)	3	PART
2	DECO,FOLDER(UPPER)	1	PART
1	COVER,FOLDER(UPPER)	1	PART

12.2 Accessories

No.	Location No.	Description	Part No.	QTY	Specification	SVC	Remark
2	MHBY00	HANDSTRAP	MHBY0001101	1	Neck Strap 400mm (CDMA,common use)	Y	
2	SSAD00	TRAVEL ADAPTOR,AC-DC	SSAD0007818	1	100-240V ,60 Hz,5.2 V,800 mA,CE ,24P	Y	
2	SGDY00	DATA CABLE	SGDY0004401	1	DK-20G, G7000 ,Cable bulk	Y	
2	SGEY00	EAR PHONE/EAR MIKE SET	SGEY0002901	1	G7000,G5200 Common use, 3P EAR MIC	Y	

12.3 Replacement part list
< Mechanic Components >

Level	Location No	Description	Part No	QTY	SPECIFICATION	svc	Remark
3	ABGA00	BUTTON ASSY, DIAL	ABGA0001901	1	Please refer to the "Exploded view"	Y	36
3	ACGG00	COVER ASSY, FOLDER	ACGG0026001	1	COVER ASSY, FOLDER	Y	
4	ACGH00	COVER ASSY, FOLDER(LOWER)	ACGH0013501	1	Please refer to the "Exploded view"	Y	
5	MCJH00	COVER, FOLDER(LOWER)	MCJH0010701	1	Please refer to the "Exploded view"	Y	18
5	MDAH00	DECO, RECEIVER	MDAH0002901	1	Please refer to the "Exploded view"	Y	20
5	MMAA00	MAGNET, SWITCH	MMAA0000601	1	Please refer to the "Exploded view"	Y	17
5	MPBG00	PAD, LCD	MPBG0012001	1	Please refer to the "Exploded view"	Y	16
5	MTAA00	TAPE, DECO	MTAA0028101	1	Please refer to the "Exploded view"	Y	19
5	MTAD00	TAPE, WINDOW	MTAD0014001	1	Please refer to the "Exploded view"	Y	22
5	MGAD00	GASKET SHIELD FOAM	MGAD0033001	1	GASKET SHIELD FOAM	Y	
4	ACGJ00	COVER ASSY, FOLDER(UPPER)	ACGJ0021501	1	COVER ASSY, FOLDER(UPPER)	Y	
5	MCJJ00	COVER, FOLDER(UPPER)	MCJJ0015101	1	Please refer to the "Exploded view"	N	1
5	MDAE00	DECO, FOLDER(UPPER)	MDAE0014401	1	Please refer to the "Exploded view"	N	2
5	MDAM00	DECO, WINDOW(SUB)	MDAM0002901	1	Please refer to the "Exploded view"	N	7
5	MICA00	INSERT, FRONT	MICA0006001	3	Please refer to the "Exploded view"	N	3
5	MPBJ00	PAD, MOTOR	MPBJ0008501	1	Please refer to the "Exploded view"	Y	9
5	MPBM00	PAD, RECEIVER	MPBM0003401	1	Please refer to the "Exploded view"	Y	10
5	MPBQ00	PAD, LCD(SUB)	MPBQ0008601	1	Please refer to the "Exploded view"	Y	11
5	MTAA00	TAPE, DECO	MTAA0028001	1	Please refer to the "Exploded view"	Y	5
5	MTAE00	TAPE, WINDOW(SUB)	MTAE0008501	1	Please refer to the "Exploded view"	Y	4
4	ACGK00	COVER ASSY, FRONT	ACGK0023501	1	COVER ASSY, FRONT	Y	
5	ABGC00	BUTTON ASSY, SIDE	ABGC0003501	1	Please refer to the "Exploded view"	Y	30
5	MBHY00	BUMPER	MBHY0003507	2	Please refer to the "Exploded view"	Y	29
5	MCJK00	COVER, FRONT	MCJK0015901	1	Please refer to the "Exploded view"	Y	28
5	MDAJ00	DECO, HINGE	MDAJ0003401	1	Please refer to the "Exploded view"	Y	33
5	MDAJ00	DECO, HINGE	MDAJ0003501	1	Please refer to the "Exploded view"	Y	32
5	MICA00	INSERT, FRONT	MICA0006001	6	Please refer to the "Exploded view"	N	34
5	MSGB00	STOPPER, HINGE	MSGB0003501	1	Please refer to the "Exploded view"	N	35
4	ALAY00	LCD, ASSY	ALAY0005701	1	Please refer to the "Exploded view"	Y	13
5	SACY00	PCB ASSY, FLEXIBLE	SACY0010001	1	G7030 MAIN TO LCD FPCB	Y	
6	ENBY00	CONNECTOR, BOARD TO BOARD	ENBY0013401	1	34 PIN, 0.4 mm	Y	
6	SPCY00	PCB, FLEXIBLE	SPCY0017101	1	POLYI, 0.3 mm, DOUBLE	Y	
5	SBCL00	BATTERY, CELL, LITHIUM	SBCL0001001	1	3V, 1.2mAh, COIN	Y	
5	SVLM00	LCD MODULE	SVLM0005501	1	128X 160, 34X 54, G7030 LCD ASS'Y	Y	

Level	Location No	Description	Part No	QTY	SPECIFICATION	svc	Remark
4	GMZZ00	SCREW MACHINE	GMZZ0009401	3	Please refer to the "Exploded view"	Y	
4	MCCH00	CAP, SCREW	MCCH0002107	2	Please refer to the "Exploded view"	Y	27
4	MCCH00	CAP, SCREW	MCCH0014601	2	Please refer to the "Exploded view"	Y	26
4	MHFD00	HINGE, FOLDER	MHFD0003301	1	Please refer to the "Exploded view"	Y	21
4	MWAC00	WINDOW, LCD	MWAC0027401	1	Please refer to the "Exploded view"	Y	23
4	MWAF00	WINDOW, LCD(SUB)	MWAF0010601	1	Please refer to the "Exploded view"	Y	6
4	SJMY00	VIBRATOR, MOTOR	SJMY0002801	1	Please refer to the "Exploded view"	Y	14
4	SUSY00	SPEAKER	SUSY0006202	1	Please refer to the "Exploded view"	Y	15
4	MPBZ00	PAD	MPBZ00027401	1	Please refer to the "Exploded view"	Y	
4	MGAD00	GASKET SHIELD FOAM	MGAD0029301	2	Please refer to the "Exploded view"	Y	12
4	MGAD00	GASKET SHIELD FOAM	MGAD0032701	1	LCD FPCB	Y	
4	MTAB00	TAPE, PROTECTION	MTAB0001401	1	Please refer to the "Exploded view"	N	8
4	MTAB00	TAPE, PROTECTION	MTAB0018201	1	Please refer to the "Exploded view"	N	24
3	ACGM00	COVER ASSY, REAR	ACGM0020001	1	COVER ASSY, REAR	Y	
4	GMZZ00	SCREW MACHINE	GMZZ0009401	1	Please refer to the "Exploded view"	Y	46
4	MCCC00	CAP, EARPHONE	MCCC0008801	1	Please refer to the "Exploded view"	Y	39
4	MCIA00	CONTACT, ANTENNA	MCIA0007301	1	Please refer to the "Exploded view"	Y	47
4	MCJN00	COVER, REAR	MCJN0013201	1	Please refer to the "Exploded view"	N	41
4	MGAD00	GASKET SHIELD FOAM	MGAD0027301	1	Please refer to the "Exploded view"	Y	40
4	MGAD00	GASKET SHIELD FOAM	MGAD0027401	1	Please refer to the "Exploded view"	Y	42
4	MICA00	INSERT, FRONT	MICA0006001	1	-	N	
4	MLEA00	LOCKER, BATTERY	MLEA0010201	1	Please refer to the "Exploded view"	Y	44
4	MSDB00	SPRING COIL	MSDB0001701	1	Please refer to the "Exploded view"	Y	43
4	MWAG00	WINDOW, IRDA	MWAG0002801	1	Please refer to the "Exploded view"	Y	30
4	SNGF00	ANTENNA, GSM, FIXED	SNGF0001801	1	Please refer to the "Exploded view"	Y	45
4	MTAB00	TAPE, PROTECTION	MTAB0020202	1	-	N	
3	ADCA00	DOME ASSY, METAL	ADCA0011901	1	Please refer to the "Exploded view"	Y	37
3	GMZZ00	SCREW MACHINE	GMZZ0009401	6	Please refer to the "Exploded view"	Y	48
3	MCCF00	CAP, MOBILE SWITCH	MCCF0009801	1	Please refer to the "Exploded view"	Y	50
3	MCCH00	CAP, SCREW	MCCH0014801	2	Please refer to the "Exploded view"	Y	49
3	MLAK00	LABEL, MODEL	MLAK0006301	1	-	Y	
3	SAFY00	PCB ASSY, MAIN	SAFY0066601	1	G7030	Y	
3	CN2	PCB ASSY, SIDE KEY	SAKY0002301	1	G7030	Y	
3	MIC1	MICROPHONE	SUMY0004101	1	FPCB, -42 dB, 6* 1.3, G5200 C-MIC	Y	
2	SBPL00	BATTERY PACK,LI-ION	SBPL0065853	1	443450(SV),3.7 V,720 mAh,1 CELL,SV	Y	

12.3 Replacement part list

< Main PCB >

Level	Location No.	Description	Part No.	Qty	Specification	SVC
3	SAFY00	PCB ASSY,MAIN	SAFY0066601	1	G7030(EUA)	Y
4	SAFA00	PCB ASSY,MAIN,AUTO	SAFA0023001	1	G7030(EUA)	N
5	C12	CAP,CERAMIC,CHIP	ECCH0000102	1	1 pF,50V,C,NP0,TC,1005,R/TP	Y
5	C33	CAP,CERAMIC,CHIP	ECCH0000103	1	1.5 pF,50V,C,NP0,TC,1005,R/TP	Y
5	C34	CAP,CERAMIC,CHIP	ECCH0000103	1	1.5 pF,50V,C,NP0,TC,1005,R/TP	Y
5	C44	CAP,CERAMIC,CHIP	ECCH0000110	1	10 pF,50V,D,NP0,TC,1005,R/TP	Y
5	C47	CAP,CERAMIC,CHIP	ECCH0000110	1	10 pF,50V,D,NP0,TC,1005,R/TP	Y
5	C49	CAP,CERAMIC,CHIP	ECCH0000110	1	10 pF,50V,D,NP0,TC,1005,R/TP	Y
5	C97	CAP,CERAMIC,CHIP	ECCH0000113	1	18 pF,50V,J,NP0,TC,1005,R/TP	Y
5	C121	CAP,CERAMIC,CHIP	ECCH0000114	1	20 pF,50V,J,NP0,TC,1005,R/TP	Y
5	C122	CAP,CERAMIC,CHIP	ECCH0000114	1	20 pF,50V,J,NP0,TC,1005,R/TP	Y
5	C53	CAP,CERAMIC,CHIP	ECCH0000115	1	22 pF,50V,J,NP0,TC,1005,R/TP	Y
5	C55	CAP,CERAMIC,CHIP	ECCH0000115	1	22 pF,50V,J,NP0,TC,1005,R/TP	Y
5	C24	CAP,CERAMIC,CHIP	ECCH0000117	1	27 pF,50V,J,NP0,TC,1005,R/TP	Y
5	C29	CAP,CERAMIC,CHIP	ECCH0000117	1	27 pF,50V,J,NP0,TC,1005,R/TP	Y
5	C51	CAP,CERAMIC,CHIP	ECCH0000117	1	27 pF,50V,J,NP0,TC,1005,R/TP	Y
5	C100	CAP,CERAMIC,CHIP	ECCH0000122	1	47 pF,50V,J,NP0,TC,1005,R/TP	Y
5	C101	CAP,CERAMIC,CHIP	ECCH0000122	1	47 pF,50V,J,NP0,TC,1005,R/TP	Y
5	C102	CAP,CERAMIC,CHIP	ECCH0000122	1	47 pF,50V,J,NP0,TC,1005,R/TP	Y
5	C135	CAP,CERAMIC,CHIP	ECCH0000122	1	47 pF,50V,J,NP0,TC,1005,R/TP	Y
5	C151	CAP,CERAMIC,CHIP	ECCH0000122	1	47 pF,50V,J,NP0,TC,1005,R/TP	Y
5	C153	CAP,CERAMIC,CHIP	ECCH0000122	1	47 pF,50V,J,NP0,TC,1005,R/TP	Y
5	C154	CAP,CERAMIC,CHIP	ECCH0000122	1	47 pF,50V,J,NP0,TC,1005,R/TP	Y
5	C155	CAP,CERAMIC,CHIP	ECCH0000122	1	47 pF,50V,J,NP0,TC,1005,R/TP	Y
5	C50	CAP,CERAMIC,CHIP	ECCH0000128	1	100 pF,50V,J,NP0,TC,1005,R/TP	Y
5	C58	CAP,CERAMIC,CHIP	ECCH0000128	1	100 pF,50V,J,NP0,TC,1005,R/TP	Y
5	C65	CAP,CERAMIC,CHIP	ECCH0000130	1	150 pF,50V,J,SL,TC,1005,R/TP	Y
5	C140	CAP,CERAMIC,CHIP	ECCH0000130	1	150 pF,50V,J,SL,TC,1005,R/TP	Y
5	C148	CAP,CERAMIC,CHIP	ECCH0000130	1	150 pF,50V,J,SL,TC,1005,R/TP	Y
5	C168	CAP,CERAMIC,CHIP	ECCH0000130	1	150 pF,50V,J,SL,TC,1005,R/TP	Y
5	C70	CAP,CERAMIC,CHIP	ECCH0000139	1	470 pF,50V,K,X7R,HD,1005,R/TP	Y
5	C104	CAP,CERAMIC,CHIP	ECCH0000139	1	470 pF,50V,K,X7R,HD,1005,R/TP	Y
5	C6	CAP,CERAMIC,CHIP	ECCH0000143	1	1 nF,50V,K,X7R,HD,1005,R/TP	Y
5	C16	CAP,CERAMIC,CHIP	ECCH0000143	1	1 nF,50V,K,X7R,HD,1005,R/TP	Y
5	C54	CAP,CERAMIC,CHIP	ECCH0000143	1	1 nF,50V,K,X7R,HD,1005,R/TP	Y
5	C57	CAP,CERAMIC,CHIP	ECCH0000143	1	1 nF,50V,K,X7R,HD,1005,R/TP	Y
5	C61	CAP,CERAMIC,CHIP	ECCH0000143	1	1 nF,50V,K,X7R,HD,1005,R/TP	Y

Level	Location No.	Description	Part No.	Qty	Specification	SVC
5	C63	CAP,CERAMIC,CHIP	ECCH0000143	1	1 nF,50V,K,X7R,HD,1005,R/TP	Y
5	C68	CAP,CERAMIC,CHIP	ECCH0000143	1	1 nF,50V,K,X7R,HD,1005,R/TP	Y
5	C71	CAP,CERAMIC,CHIP	ECCH0000143	1	1 nF,50V,K,X7R,HD,1005,R/TP	Y
5	C82	CAP,CERAMIC,CHIP	ECCH0000143	1	1 nF,50V,K,X7R,HD,1005,R/TP	Y
5	C91	CAP,CERAMIC,CHIP	ECCH0000143	1	1 nF,50V,K,X7R,HD,1005,R/TP	Y
5	C92	CAP,CERAMIC,CHIP	ECCH0000143	1	1 nF,50V,K,X7R,HD,1005,R/TP	Y
5	C159	CAP,CERAMIC,CHIP	ECCH0000143	1	1 nF,50V,K,X7R,HD,1005,R/TP	Y
5	C52	CAP,CERAMIC,CHIP	ECCH0000149	1	3.3 nF,50V,K,X7R,HD,1005,R/TP	Y
5	C147	CAP,CERAMIC,CHIP	ECCH0000159	1	22 nF,16V,K,X7R,HD,1005,R/TP	Y
5	C76	CAP,CERAMIC,CHIP	ECCH0000161	1	33 nF,16V,K,X7R,HD,1005,R/TP	Y
5	C138	CAP,CERAMIC,CHIP	ECCH0000161	1	33 nF,16V,K,X7R,HD,1005,R/TP	Y
5	C37	CAP,CERAMIC,CHIP	ECCH0000179	1	22 nF,16V ,K ,X5R ,HD ,1005 ,R/TP	Y
5	C39	CAP,CERAMIC,CHIP	ECCH0000179	1	22 nF,16V ,K ,X5R ,HD ,1005 ,R/TP	Y
5	C40	CAP,CERAMIC,CHIP	ECCH0000179	1	22 nF,16V ,K ,X5R ,HD ,1005 ,R/TP	Y
5	C41	CAP,CERAMIC,CHIP	ECCH0000179	1	22 nF,16V ,K ,X5R ,HD ,1005 ,R/TP	Y
5	C43	CAP,CERAMIC,CHIP	ECCH0000179	1	22 nF,16V ,K ,X5R ,HD ,1005 ,R/TP	Y
5	C56	CAP,CERAMIC,CHIP	ECCH0000179	1	22 nF,16V ,K ,X5R ,HD ,1005 ,R/TP	Y
5	C60	CAP,CERAMIC,CHIP	ECCH0000179	1	22 nF,16V ,K ,X5R ,HD ,1005 ,R/TP	Y
5	C62	CAP,CERAMIC,CHIP	ECCH0000179	1	22 nF,16V ,K ,X5R ,HD ,1005 ,R/TP	Y
5	C160	CAP,CERAMIC,CHIP	ECCH0000179	1	22 nF,16V ,K ,X5R ,HD ,1005 ,R/TP	Y
5	C8	CAP,CERAMIC,CHIP	ECCH0000182	1	0.1 uF,10V ,K ,X5R ,HD ,1005 ,R/TP	Y
5	C13	CAP,CERAMIC,CHIP	ECCH0000182	1	0.1 uF,10V ,K ,X5R ,HD ,1005 ,R/TP	Y
5	C15	CAP,CERAMIC,CHIP	ECCH0000182	1	0.1 uF,10V ,K ,X5R ,HD ,1005 ,R/TP	Y
5	C25	CAP,CERAMIC,CHIP	ECCH0000182	1	0.1 uF,10V ,K ,X5R ,HD ,1005 ,R/TP	Y
5	C26	CAP,CERAMIC,CHIP	ECCH0000182	1	0.1 uF,10V ,K ,X5R ,HD ,1005 ,R/TP	Y
5	C27	CAP,CERAMIC,CHIP	ECCH0000182	1	0.1 uF,10V ,K ,X5R ,HD ,1005 ,R/TP	Y
5	C73	CAP,CERAMIC,CHIP	ECCH0000182	1	0.1 uF,10V ,K ,X5R ,HD ,1005 ,R/TP	Y
5	C74	CAP,CERAMIC,CHIP	ECCH0000182	1	0.1 uF,10V ,K ,X5R ,HD ,1005 ,R/TP	Y
5	C81	CAP,CERAMIC,CHIP	ECCH0000182	1	0.1 uF,10V ,K ,X5R ,HD ,1005 ,R/TP	Y
5	C84	CAP,CERAMIC,CHIP	ECCH0000182	1	0.1 uF,10V ,K ,X5R ,HD ,1005 ,R/TP	Y
5	C86	CAP,CERAMIC,CHIP	ECCH0000182	1	0.1 uF,10V ,K ,X5R ,HD ,1005 ,R/TP	Y
5	C87	CAP,CERAMIC,CHIP	ECCH0000182	1	0.1 uF,10V ,K ,X5R ,HD ,1005 ,R/TP	Y
5	C95	CAP,CERAMIC,CHIP	ECCH0000182	1	0.1 uF,10V ,K ,X5R ,HD ,1005 ,R/TP	Y
5	C96	CAP,CERAMIC,CHIP	ECCH0000182	1	0.1 uF,10V ,K ,X5R ,HD ,1005 ,R/TP	Y
5	C98	CAP,CERAMIC,CHIP	ECCH0000182	1	0.1 uF,10V ,K ,X5R ,HD ,1005 ,R/TP	Y
5	C99	CAP,CERAMIC,CHIP	ECCH0000182	1	0.1 uF,10V ,K ,X5R ,HD ,1005 ,R/TP	Y
5	C109	CAP,CERAMIC,CHIP	ECCH0000182	1	0.1 uF,10V ,K ,X5R ,HD ,1005 ,R/TP	Y
5	C111	CAP,CERAMIC,CHIP	ECCH0000182	1	0.1 uF,10V ,K ,X5R ,HD ,1005 ,R/TP	Y
5	C123	CAP,CERAMIC,CHIP	ECCH0000182	1	0.1 uF,10V ,K ,X5R ,HD ,1005 ,R/TP	Y
5	C128	CAP,CERAMIC,CHIP	ECCH0000182	1	0.1 uF,10V ,K ,X5R ,HD ,1005 ,R/TP	Y

Level	Location No.	Description	Part No.	Qty	Specification	SVC
5	C129	CAP,CERAMIC,CHIP	ECCH0000182	1	0.1 uF,10V ,K ,X5R ,HD ,1005 ,R/TP	Y
5	C137	CAP,CERAMIC,CHIP	ECCH0000182	1	0.1 uF,10V ,K ,X5R ,HD ,1005 ,R/TP	Y
5	C139	CAP,CERAMIC,CHIP	ECCH0000182	1	0.1 uF,10V ,K ,X5R ,HD ,1005 ,R/TP	Y
5	C141	CAP,CERAMIC,CHIP	ECCH0000182	1	0.1 uF,10V ,K ,X5R ,HD ,1005 ,R/TP	Y
5	C146	CAP,CERAMIC,CHIP	ECCH0000182	1	0.1 uF,10V ,K ,X5R ,HD ,1005 ,R/TP	Y
5	C150	CAP,CERAMIC,CHIP	ECCH0000182	1	0.1 uF,10V ,K ,X5R ,HD ,1005 ,R/TP	Y
5	C152	CAP,CERAMIC,CHIP	ECCH0000182	1	0.1 uF,10V ,K ,X5R ,HD ,1005 ,R/TP	Y
5	C156	CAP,CERAMIC,CHIP	ECCH0000182	1	0.1 uF,10V ,K ,X5R ,HD ,1005 ,R/TP	Y
5	C157	CAP,CERAMIC,CHIP	ECCH0000182	1	0.1 uF,10V ,K ,X5R ,HD ,1005 ,R/TP	Y
5	C164	CAP,CERAMIC,CHIP	ECCH0000182	1	0.1 uF,10V ,K ,X5R ,HD ,1005 ,R/TP	Y
5	C167	CAP,CERAMIC,CHIP	ECCH0000182	1	0.1 uF,10V ,K ,X5R ,HD ,1005 ,R/TP	Y
5	C1	CAP,CERAMIC,CHIP	ECCH0000186	1	33 pF,50V ,J ,NP0 ,TC ,1005 ,R/TP	Y
5	C2	CAP,CERAMIC,CHIP	ECCH0000186	1	33 pF,50V ,J ,NP0 ,TC ,1005 ,R/TP	Y
5	C3	CAP,CERAMIC,CHIP	ECCH0000186	1	33 pF,50V ,J ,NP0 ,TC ,1005 ,R/TP	Y
5	C4	CAP,CERAMIC,CHIP	ECCH0000186	1	33 pF,50V ,J ,NP0 ,TC ,1005 ,R/TP	Y
5	C5	CAP,CERAMIC,CHIP	ECCH0000186	1	33 pF,50V ,J ,NP0 ,TC ,1005 ,R/TP	Y
5	C7	CAP,CERAMIC,CHIP	ECCH0000186	1	33 pF,50V ,J ,NP0 ,TC ,1005 ,R/TP	Y
5	C17	CAP,CERAMIC,CHIP	ECCH0000186	1	33 pF,50V ,J ,NP0 ,TC ,1005 ,R/TP	Y
5	C18	CAP,CERAMIC,CHIP	ECCH0000186	1	33 pF,50V ,J ,NP0 ,TC ,1005 ,R/TP	Y
5	C19	CAP,CERAMIC,CHIP	ECCH0000186	1	33 pF,50V ,J ,NP0 ,TC ,1005 ,R/TP	Y
5	C20	CAP,CERAMIC,CHIP	ECCH0000186	1	33 pF,50V ,J ,NP0 ,TC ,1005 ,R/TP	Y
5	C21	CAP,CERAMIC,CHIP	ECCH0000186	1	33 pF,50V ,J ,NP0 ,TC ,1005 ,R/TP	Y
5	C22	CAP,CERAMIC,CHIP	ECCH0000186	1	33 pF,50V ,J ,NP0 ,TC ,1005 ,R/TP	Y
5	C23	CAP,CERAMIC,CHIP	ECCH0000186	1	33 pF,50V ,J ,NP0 ,TC ,1005 ,R/TP	Y
5	C48	CAP,CERAMIC,CHIP	ECCH0000186	1	33 pF,50V ,J ,NP0 ,TC ,1005 ,R/TP	Y
5	C105	CAP,CERAMIC,CHIP	ECCH0000186	1	33 pF,50V ,J ,NP0 ,TC ,1005 ,R/TP	Y
5	C106	CAP,CERAMIC,CHIP	ECCH0000186	1	33 pF,50V ,J ,NP0 ,TC ,1005 ,R/TP	Y
5	C107	CAP,CERAMIC,CHIP	ECCH0000186	1	33 pF,50V ,J ,NP0 ,TC ,1005 ,R/TP	Y
5	C108	CAP,CERAMIC,CHIP	ECCH0000186	1	33 pF,50V ,J ,NP0 ,TC ,1005 ,R/TP	Y
5	C113	CAP,CERAMIC,CHIP	ECCH0000186	1	33 pF,50V ,J ,NP0 ,TC ,1005 ,R/TP	Y
5	C114	CAP,CERAMIC,CHIP	ECCH0000186	1	33 pF,50V ,J ,NP0 ,TC ,1005 ,R/TP	Y
5	C115	CAP,CERAMIC,CHIP	ECCH0000186	1	33 pF,50V ,J ,NP0 ,TC ,1005 ,R/TP	Y
5	C116	CAP,CERAMIC,CHIP	ECCH0000186	1	33 pF,50V ,J ,NP0 ,TC ,1005 ,R/TP	Y
5	C117	CAP,CERAMIC,CHIP	ECCH0000186	1	33 pF,50V ,J ,NP0 ,TC ,1005 ,R/TP	Y
5	C118	CAP,CERAMIC,CHIP	ECCH0000186	1	33 pF,50V ,J ,NP0 ,TC ,1005 ,R/TP	Y
5	C119	CAP,CERAMIC,CHIP	ECCH0000186	1	33 pF,50V ,J ,NP0 ,TC ,1005 ,R/TP	Y
5	C124	CAP,CERAMIC,CHIP	ECCH0000186	1	33 pF,50V ,J ,NP0 ,TC ,1005 ,R/TP	Y
5	C125	CAP,CERAMIC,CHIP	ECCH0000186	1	33 pF,50V ,J ,NP0 ,TC ,1005 ,R/TP	Y
5	C126	CAP,CERAMIC,CHIP	ECCH0000186	1	33 pF,50V ,J ,NP0 ,TC ,1005 ,R/TP	Y
5	C142	CAP,CERAMIC,CHIP	ECCH0000186	1	33 pF,50V ,J ,NP0 ,TC ,1005 ,R/TP	Y

Level	Location No.	Description	Part No.	Qty	Specification	SVC
5	C144	CAP,CERAMIC,CHIP	ECCH0000186	1	33 pF,50V ,J ,NP0 ,TC ,1005 ,R/TP	Y
5	C145	CAP,CERAMIC,CHIP	ECCH0000186	1	33 pF,50V ,J ,NP0 ,TC ,1005 ,R/TP	Y
5	C85	CAP,CERAMIC,CHIP	ECCH0000276	1	1 uF,10V,Z,Y5V,HD,1608,R/TP	Y
5	C93	CAP,CERAMIC,CHIP	ECCH0000276	1	1 uF,10V,Z,Y5V,HD,1608,R/TP	Y
5	C112	CAP,CERAMIC,CHIP	ECCH0000276	1	1 uF,10V,Z,Y5V,HD,1608,R/TP	Y
5	C127	CAP,CERAMIC,CHIP	ECCH0000276	1	1 uF,10V,Z,Y5V,HD,1608,R/TP	Y
5	C136	CAP,CERAMIC,CHIP	ECCH0000276	1	1 uF,10V,Z,Y5V,HD,1608,R/TP	Y
5	C143	CAP,CERAMIC,CHIP	ECCH0000276	1	1 uF,10V,Z,Y5V,HD,1608,R/TP	Y
5	C163	CAP,CERAMIC,CHIP	ECCH0000276	1	1 uF,10V,Z,Y5V,HD,1608,R/TP	Y
5	C166	CAP,CERAMIC,CHIP	ECCH0000276	1	1 uF,10V,Z,Y5V,HD,1608,R/TP	Y
5	C35	CAP,CERAMIC,CHIP	ECCH0000701	1	1.2 pF,50V ,C ,NP0 ,TC ,1005 ,R/TP	Y
5	C36	CAP,CERAMIC,CHIP	ECCH0000701	1	1.2 pF,50V ,C ,NP0 ,TC ,1005 ,R/TP	Y
5	C64	CAP,CERAMIC,CHIP	ECCH0003401	1	10 uF,6.3V ,Z ,Y5V ,HD ,2012 ,R/TP	Y
5	C69	CAP,CERAMIC,CHIP	ECCH0003401	1	10 uF,6.3V ,Z ,Y5V ,HD ,2012 ,R/TP	Y
5	C72	CAP,CERAMIC,CHIP	ECCH0003401	1	10 uF,6.3V ,Z ,Y5V ,HD ,2012 ,R/TP	Y
5	C75	CAP,CERAMIC,CHIP	ECCH0003401	1	10 uF,6.3V ,Z ,Y5V ,HD ,2012 ,R/TP	Y
5	C83	CAP,CERAMIC,CHIP	ECCH0003401	1	10 uF,6.3V ,Z ,Y5V ,HD ,2012 ,R/TP	Y
5	C94	CAP,CERAMIC,CHIP	ECCH0003401	1	10 uF,6.3V ,Z ,Y5V ,HD ,2012 ,R/TP	Y
5	C130	CAP,CERAMIC,CHIP	ECCH0003401	1	10 uF,6.3V ,Z ,Y5V ,HD ,2012 ,R/TP	Y
5	C132	CAP,CERAMIC,CHIP	ECCH0003401	1	10 uF,6.3V ,Z ,Y5V ,HD ,2012 ,R/TP	Y
5	C149	CAP,CERAMIC,CHIP	ECCH0003401	1	10 uF,6.3V ,Z ,Y5V ,HD ,2012 ,R/TP	Y
5	C169	CAP,CERAMIC,CHIP	ECCH0003401	1	10 uF,6.3V ,Z ,Y5V ,HD ,2012 ,R/TP	Y
5	C170	CAP,CERAMIC,CHIP	ECCH0003401	1	10 uF,6.3V ,Z ,Y5V ,HD ,2012 ,R/TP	Y
5	C133	CAP,CERAMIC,CHIP	ECCH0003803	1	4.7 uF,10V ,Z ,Y5V ,HD ,2012 ,R/TP	Y
5	C134	CAP,CERAMIC,CHIP	ECCH0003803	1	4.7 uF,10V ,Z ,Y5V ,HD ,2012 ,R/TP	Y
5	C88	CAP,CERAMIC,CHIP	ECCH0004902	1	220 nF,10V ,Z ,Y5V ,TC ,1005 ,R/TP	Y
5	C59	CAP,TANTAL,CHIP,MAKER	ECTZ0003901	1	595D106X0016A2T,10 uF,16V ,M ,STD ,ETC ,R/TP	Y
5	LD2	DIODE,LED,CHIP	EDLH0004502	1	LEBB-S14H,BLUE ,1608 ,R/TP ,0.35T	Y
5	LD4	DIODE,LED,CHIP	EDLH0004502	1	LEBB-S14H,BLUE ,1608 ,R/TP ,0.35T	Y
5	LD5	DIODE,LED,CHIP	EDLH0004502	1	LEBB-S14H,BLUE ,1608 ,R/TP ,0.35T	Y
5	LD6	DIODE,LED,CHIP	EDLH0004502	1	LEBB-S14H,BLUE ,1608 ,R/TP ,0.35T	Y
5	LD7	DIODE,LED,CHIP	EDLH0004502	1	LEBB-S14H,BLUE ,1608 ,R/TP ,0.35T	Y
5	LD8	DIODE,LED,CHIP	EDLH0004502	1	LEBB-S14H,BLUE ,1608 ,R/TP ,0.35T	Y
5	LD9	DIODE,LED,CHIP	EDLH0004502	1	LEBB-S14H,BLUE ,1608 ,R/TP ,0.35T	Y
5	LD10	DIODE,LED,CHIP	EDLH0004502	1	LEBB-S14H,BLUE ,1608 ,R/TP ,0.35T	Y
5	LD11	DIODE,LED,CHIP	EDLH0004502	1	LEBB-S14H,BLUE ,1608 ,R/TP ,0.35T	Y
5	LD12	DIODE,LED,CHIP	EDLH0004502	1	LEBB-S14H,BLUE ,1608 ,R/TP ,0.35T	Y
5	LD13	DIODE,LED,CHIP	EDLH0004502	1	LEBB-S14H,BLUE ,1608 ,R/TP ,0.35T	Y
5	LD15	DIODE,LED,CHIP	EDLH0004502	1	LEBB-S14H,BLUE ,1608 ,R/TP ,0.35T	Y
5	D5	DIODE,SWITCHING	EDSY0005201	1	CRS08(TE85L),SMD ,30 V,1.5 A,R/TP ,	Y

Level	Location No.	Description	Part No.	Qty	Specification	SVC
5	D2	DIODE,SWITCHING	EDSY0010401	1	1SS388,1-1G1A ,40 V,300 A,R/TP ,Silicon Epitaxial Schottky Barrier Type Diode	Y
5	D3	DIODE,SWITCHING	EDSY0010401	1	1SS388,1-1G1A ,40 V,300 A,R/TP ,Silicon Epitaxial Schottky Barrier Type Diode	Y
5	D4	DIODE,SWITCHING	EDSY0010401	1	1SS388,1-1G1A ,40 V,300 A,R/TP ,Silicon Epitaxial Schottky Barrier Type Diode	Y
5	D6	DIODE,SWITCHING	EDSY0010401	1	1SS388,1-1G1A ,40 V,300 A,R/TP ,Silicon Epitaxial Schottky Barrier Type Diode	Y
5	L5	INDUCTOR,CHIP	ELCH0000739	1	0603AS-022J-01,22 nH,J ,1608 ,R/TP ,	Y
5	L6	INDUCTOR,CHIP	ELCH0000749	1	0603AS-5N6J,5.6 nH,J ,1608 ,R/TP ,	Y
5	L7	INDUCTOR,CHIP	ELCH0001406	1	LL1005-FH4N7S,4.7 nH,S,1005,R/TP	Y
5	L10	INDUCTOR,CHIP	ELCH0001408	1	LL1005-FH6N8J,6.8 nH,J ,1005 ,R/TP ,	Y
5	L17	INDUCTOR,CHIP	ELCH0001413	1	LL1005-FH22NJ,22 nH,J ,1005 ,R/TP ,	Y
5	L11	INDUCTOR,CHIP	ELCH0001426	1	LL1005-FH8N2J,8.2 nH,J ,1005 ,R/TP ,	Y
5	L18	INDUCTOR,CHIP	ELCH0001427	1	LL1005-FH2N2S,2.2 nH,S ,1005 ,R/TP ,	Y
5	L3	INDUCTOR,CHIP	ELCH0005009	1	HK1005R10J,100 nH,J ,1005 ,R/TP ,	Y
5	L12	INDUCTOR,CHIP	ELCH0005009	1	HK1005R10J,100 nH,J ,1005 ,R/TP ,	Y
5	L13	INDUCTOR,CHIP	ELCH0005009	1	HK1005R10J,100 nH,J ,1005 ,R/TP ,	Y
5	L14	INDUCTOR,CHIP	ELCH0005009	1	HK1005R10J,100 nH,J ,1005 ,R/TP ,	Y
5	L15	INDUCTOR,CHIP	ELCH0005009	1	HK1005R10J,100 nH,J ,1005 ,R/TP ,	Y
5	L16	INDUCTOR,CHIP	ELCH0005009	1	HK1005R10J,100 nH,J ,1005 ,R/TP ,	Y
5	J1	CONNECTOR,BOARD TO BOARD	ENBY0013402	1	24-5602-034-001-829,34 PIN,0.4 mm,STRAIGHT ,Au ,B to B G5400	Y
5	J3	CONN,JACK/PLUG,EARPHONE	ENJE0002301	1	KJA-PH-3-0028,3,5 PIN,G7000 EAR JACK 3 pole, 5 pin KSD	Y
5	J4	CONNECTOR,I/O	ENRY0000801	1	GT056-24P-P1000,24 PIN,0.5 mm,ANGLE ,AU GOLD ,	Y
5	J2	CONN,SOCKET	ENSY0007602	1	PC-D6-A3-H2.7-S,6 PIN,ETC , , mm,Height 2.7mm	Y
5	SW1	CONN,RF SWITCH	ENWY0000401	1	MM8430-2600B,STRAIGHT ,SMD ,0.1 dB,3*3*1.8 / 500 CYCLES	Y
5	Q3	TR,BJT,NPN	EQBN0004801	1	IMX9T110,SMT6 ,0.2 W,R/TP ,	Y
5	Q2	TR,BJT,NPN	EQBN0007001	1	RN1307(TE85L),SC-70 ,0.1 W,R/TP ,	Y
5	Q4	TR,FET,P-CHANNEL	EQFP0003301	1	NDC652P,SOT-6 ,1.6 W,30 V,2.4 A,R/TP ,use for charge P- CHANNEL FET	Y
5	R15	RES,CHIP	ERHY0000184	1	150 ohm,1/16W ,F ,1005 ,R/TP	Y
5	R21	RES,CHIP	ERHY0000184	1	150 ohm,1/16W ,F ,1005 ,R/TP	Y
5	R38	RES,CHIP	ERHY0000201	1	0 ohm,1/16W,J,1005,R/TP	Y
5	R39	RES,CHIP	ERHY0000201	1	0 ohm,1/16W,J,1005,R/TP	Y
5	R40	RES,CHIP	ERHY0000201	1	0 ohm,1/16W,J,1005,R/TP	Y
5	R41	RES,CHIP	ERHY0000201	1	0 ohm,1/16W,J,1005,R/TP	Y
5	R51	RES,CHIP	ERHY0000201	1	0 ohm,1/16W,J,1005,R/TP	Y
5	R97	RES,CHIP	ERHY0000201	1	0 ohm,1/16W,J,1005,R/TP	Y

Level	Location No.	Description	Part No.	Qty	Specification	SVC
5	R98	RES,CHIP	ERHY0000201	1	0 ohm,1/16W,J,1005,R/TP	Y
5	R106	RES,CHIP	ERHY0000201	1	0 ohm,1/16W,J,1005,R/TP	Y
5	R108	RES,CHIP	ERHY0000201	1	0 ohm,1/16W,J,1005,R/TP	Y
5	R120	RES,CHIP	ERHY0000201	1	0 ohm,1/16W,J,1005,R/TP	Y
5	R128	RES,CHIP	ERHY0000201	1	0 ohm,1/16W,J,1005,R/TP	Y
5	R129	RES,CHIP	ERHY0000201	1	0 ohm,1/16W,J,1005,R/TP	Y
5	R133	RES,CHIP	ERHY0000201	1	0 ohm,1/16W,J,1005,R/TP	Y
5	R134	RES,CHIP	ERHY0000201	1	0 ohm,1/16W,J,1005,R/TP	Y
5	R135	RES,CHIP	ERHY0000201	1	0 ohm,1/16W,J,1005,R/TP	Y
5	R136	RES,CHIP	ERHY0000201	1	0 ohm,1/16W,J,1005,R/TP	Y
5	R137	RES,CHIP	ERHY0000201	1	0 ohm,1/16W,J,1005,R/TP	Y
5	R141	RES,CHIP	ERHY0000201	1	0 ohm,1/16W,J,1005,R/TP	Y
5	R142	RES,CHIP	ERHY0000201	1	0 ohm,1/16W,J,1005,R/TP	Y
5	R82	RES,CHIP	ERHY0000202	1	4.7 ohm,1/16W,J,1005,R/TP	Y
5	R121	RES,CHIP	ERHY0000202	1	4.7 ohm,1/16W,J,1005,R/TP	Y
5	R122	RES,CHIP	ERHY0000202	1	4.7 ohm,1/16W,J,1005,R/TP	Y
5	R131	RES,CHIP	ERHY0000202	1	4.7 ohm,1/16W,J,1005,R/TP	Y
5	R14	RES,CHIP	ERHY0000206	1	18 ohm,1/16W,J,1005,R/TP	Y
5	R70	RES,CHIP	ERHY0000207	1	20 ohm,1/16W,J,1005,R/TP	Y
5	R71	RES,CHIP	ERHY0000207	1	20 ohm,1/16W,J,1005,R/TP	Y
5	R96	RES,CHIP	ERHY0000211	1	33 ohm,1/16W,J,1005,R/TP	Y
5	R131	RES,CHIP	ERHY0000211	1	33 ohm,1/16W,J,1005,R/TP	Y
5	R138	RES,CHIP	ERHY0000211	1	33 ohm,1/16W,J,1005,R/TP	Y
5	R13	RES,CHIP	ERHY0000212	1	39 ohm,1/16W,J,1005,R/TP	Y
5	R86	RES,CHIP	ERHY0000213	1	47 ohm,1/16W,J,1005,R/TP	Y
5	R16	RES,CHIP	ERHY0000220	1	100 ohm,1/16W,J,1005,R/TP	Y
5	R17	RES,CHIP	ERHY0000220	1	100 ohm,1/16W,J,1005,R/TP	Y
5	R29	RES,CHIP	ERHY0000220	1	100 ohm,1/16W,J,1005,R/TP	Y
5	R31	RES,CHIP	ERHY0000220	1	100 ohm,1/16W,J,1005,R/TP	Y
5	R123	RES,CHIP	ERHY0000220	1	100 ohm,1/16W,J,1005,R/TP	Y
5	R2	RES,CHIP	ERHY0000226	1	220 ohm,1/16W,J,1005,R/TP	Y
5	R103	RES,CHIP	ERHY0000228	1	270 ohm,1/16W,J,1005,R/TP	Y
5	R20	RES,CHIP	ERHY0000229	1	300 ohm,1/16W,J,1005,R/TP	Y
5	R23	RES,CHIP	ERHY0000229	1	300 ohm,1/16W,J,1005,R/TP	Y
5	R146	RES,CHIP	ERHY0000230	1	330 ohm,1/16W,J,1005,R/TP	Y
5	R147	RES,CHIP	ERHY0000230	1	330 ohm,1/16W,J,1005,R/TP	Y
5	R148	RES,CHIP	ERHY0000230	1	330 ohm,1/16W,J,1005,R/TP	Y
5	R149	RES,CHIP	ERHY0000230	1	330 ohm,1/16W,J,1005,R/TP	Y
5	R150	RES,CHIP	ERHY0000230	1	330 ohm,1/16W,J,1005,R/TP	Y
5	R151	RES,CHIP	ERHY0000230	1	330 ohm,1/16W,J,1005,R/TP	Y

Level	Location No.	Description	Part No.	Qty	Specification	SVC
5	R152	RES,CHIP	ERHY0000230	1	330 ohm,1/16W,J,1005,R/TP	Y
5	R153	RES,CHIP	ERHY0000230	1	330 ohm,1/16W,J,1005,R/TP	Y
5	R154	RES,CHIP	ERHY0000230	1	330 ohm,1/16W,J,1005,R/TP	Y
5	R155	RES,CHIP	ERHY0000230	1	330 ohm,1/16W,J,1005,R/TP	Y
5	R156	RES,CHIP	ERHY0000230	1	330 ohm,1/16W,J,1005,R/TP	Y
5	R157	RES,CHIP	ERHY0000230	1	330 ohm,1/16W,J,1005,R/TP	Y
5	R75	RES,CHIP	ERHY0000233	1	470 ohm,1/16W,J,1005,R/TP	Y
5	R84	RES,CHIP	ERHY0000233	1	470 ohm,1/16W,J,1005,R/TP	Y
5	R22	RES,CHIP	ERHY0000236	1	620 ohm,1/16W,J,1005,R/TP	Y
5	R24	RES,CHIP	ERHY0000236	1	620 ohm,1/16W,J,1005,R/TP	Y
5	R25	RES,CHIP	ERHY0000236	1	620 ohm,1/16W,J,1005,R/TP	Y
5	R26	RES,CHIP	ERHY0000236	1	620 ohm,1/16W,J,1005,R/TP	Y
5	R34	RES,CHIP	ERHY0000236	1	620 ohm,1/16W,J,1005,R/TP	Y
5	R64	RES,CHIP	ERHY0000236	1	620 ohm,1/16W,J,1005,R/TP	Y
5	R65	RES,CHIP	ERHY0000236	1	620 ohm,1/16W,J,1005,R/TP	Y
5	R85	RES,CHIP	ERHY0000236	1	620 ohm,1/16W,J,1005,R/TP	Y
5	R91	RES,CHIP	ERHY0000236	1	620 ohm,1/16W,J,1005,R/TP	Y
5	R92	RES,CHIP	ERHY0000236	1	620 ohm,1/16W,J,1005,R/TP	Y
5	R95	RES,CHIP	ERHY0000236	1	620 ohm,1/16W,J,1005,R/TP	Y
5	R47	RES,CHIP	ERHY0000237	1	680 ohm,1/16W,J,1005,R/TP	Y
5	R87	RES,CHIP	ERHY0000241	1	1K ohm,1/16W,J,1005,R/TP	Y
5	R119	RES,CHIP	ERHY0000241	1	1K ohm,1/16W,J,1005,R/TP	Y
5	R140	RES,CHIP	ERHY0000241	1	1K ohm,1/16W,J,1005,R/TP	Y
5	R143	RES,CHIP	ERHY0000241	1	1K ohm,1/16W,J,1005,R/TP	Y
5	R144	RES,CHIP	ERHY0000241	1	1K ohm,1/16W,J,1005,R/TP	Y
5	R74	RES,CHIP	ERHY0000243	1	1.2K ohm,1/16W,J,1005,R/TP	Y
5	R6	RES,CHIP	ERHY0000244	1	1.5K ohm,1/16W,J,1005,R/TP	Y
5	R101	RES,CHIP	ERHY0000244	1	1.5K ohm,1/16W,J,1005,R/TP	Y
5	R159	RES,CHIP	ERHY0000244	1	1.5K ohm,1/16W,J,1005,R/TP	Y
5	R83	RES,CHIP	ERHY0000247	1	2.2K ohm,1/16W,J,1005,R/TP	Y
5	R66	RES,CHIP	ERHY0000248	1	2.4K ohm,1/16W,J,1005,R/TP	Y
5	R124	RES,CHIP	ERHY0000250	1	3.3K ohm,1/16W,J,1005,R/TP	Y
5	R46	RES,CHIP	ERHY0000254	1	4.7K ohm,1/16W,J,1005,R/TP	Y
5	R67	RES,CHIP	ERHY0000254	1	4.7K ohm,1/16W,J,1005,R/TP	Y
5	R76	RES,CHIP	ERHY0000261	1	10K ohm,1/16W,J,1005,R/TP	Y
5	R93	RES,CHIP	ERHY0000261	1	10K ohm,1/16W,J,1005,R/TP	Y
5	R99	RES,CHIP	ERHY0000261	1	10K ohm,1/16W,J,1005,R/TP	Y
5	R118	RES,CHIP	ERHY0000261	1	10K ohm,1/16W,J,1005,R/TP	Y
5	R127	RES,CHIP	ERHY0000262	1	12K ohm,1/16W,J,1005,R/TP	Y
5	R19	RES,CHIP	ERHY0000263	1	15K ohm,1/16W,J,1005,R/TP	Y

Level	Location No.	Description	Part No.	Qty	Specification	SVC
5	R48	RES,CHIP	ERHY0000263	1	15K ohm,1/16W,J,1005,R/TP	Y
5	R53	RES,CHIP	ERHY0000265	1	20K ohm,1/16W,J,1005,R/TP	Y
5	R69	RES,CHIP	ERHY0000265	1	20K ohm,1/16W,J,1005,R/TP	Y
5	R102	RES,CHIP	ERHY0000265	1	20K ohm,1/16W,J,1005,R/TP	Y
5	R115	RES,CHIP	ERHY0000265	1	20K ohm,1/16W,J,1005,R/TP	Y
5	R10	RES,CHIP	ERHY0000273	1	47K ohm,1/16W,J,1005,R/TP	Y
5	R112	RES,CHIP	ERHY0000273	1	47K ohm,1/16W,J,1005,R/TP	Y
5	R49	RES,CHIP	ERHY0000280	1	100K ohm,1/16W,J,1005,R/TP	Y
5	R52	RES,CHIP	ERHY0000280	1	100K ohm,1/16W,J,1005,R/TP	Y
5	R77	RES,CHIP	ERHY0000280	1	100K ohm,1/16W,J,1005,R/TP	Y
5	R89	RES,CHIP	ERHY0000280	1	100K ohm,1/16W,J,1005,R/TP	Y
5	R100	RES,CHIP	ERHY0000280	1	100K ohm,1/16W,J,1005,R/TP	Y
5	R105	RES,CHIP	ERHY0000280	1	100K ohm,1/16W,J,1005,R/TP	Y
5	R113	RES,CHIP	ERHY0000280	1	100K ohm,1/16W,J,1005,R/TP	Y
5	R158	RES,CHIP	ERHY0000280	1	100K ohm,1/16W,J,1005,R/TP	Y
5	R90	RES,CHIP	ERHY0000282	1	120K ohm,1/16W,J,1005,R/TP	Y
5	R60	RES,CHIP	ERHY0000287	1	220K ohm,1/16W,J,1005,R/TP	Y
5	R88	RES,CHIP	ERHY0000287	1	220K ohm,1/16W,J,1005,R/TP	Y
5	R37	RES,CHIP	ERHY0000289	1	270K ohm,1/16W,J,1005,R/TP	Y
5	R1	RES,CHIP	ERHY0000296	1	1M ohm,1/16W,J,1005,R/TP	Y
5	R27	RES,CHIP	ERHY0000296	1	1M ohm,1/16W,J,1005,R/TP	Y
5	R62	RES,CHIP	ERHY0000296	1	1M ohm,1/16W,J,1005,R/TP	Y
5	R80	RES,CHIP	ERHY0000296	1	1M ohm,1/16W,J,1005,R/TP	Y
5	R114	RES,CHIP	ERHY0000299	1	33000 ohm,1/16W ,J ,1005 ,R/TP	Y
5	R117	RES,CHIP	ERHY0000299	1	33000 ohm,1/16W ,J ,1005 ,R/TP	Y
5	R126	RES,CHIP	ERHY0001102	1	0.2 ohm,1/4W ,F ,2012 ,R/TP	Y
5	RA1	RES,ARRAY,R	ERNR0000401	1	MNR04M0ABJ470,47 ohm, ohm,8 PIN,J ,1/32 W ,SMD ,R/TP	Y
5	RA4	RES,ARRAY,R	ERNR0000401	1	MNR04M0ABJ470,47 ohm, ohm,8 PIN,J ,1/32 W ,SMD ,R/TP	Y
5	R116	RES,ARRAY,R	ERNR0000403	1	MNR04M0ABJ103,10000 ohm, ohm,8 PIN,J ,1/32 W ,SMD ,R/TP	Y
5	V1	RES,VARIABLE,ETC	ERVZ0000101	1	AVL5M02-200,ohm, PIN, ,SMD ,R/TP ,1005 SIZE CHIP VARISTOR	Y
5	VA5	RES,VARIABLE,ETC	ERVZ0000101	1	AVL5M02-200,ohm, PIN, ,SMD ,R/TP ,1005 SIZE CHIP VARISTOR	Y
5	VA6	RES,VARIABLE,ETC	ERVZ0000101	1	AVL5M02-200,ohm, PIN, ,SMD ,R/TP ,1005 SIZE CHIP VARISTOR	Y
5	U9	IC	EUSY0076701	1	ADP3330-2.85-R,SOT-23-6 ,6 PIN,R/TP ,	Y
5	U8	IC	EUSY0077201	1	SN74AHC1GU04DCKR,SOT(DCK) ,5 PIN,R/TP ,	Y
5	U20	IC	EUSY0077301	1	MAX4599EXT-T,SC70-6/SOT23-6 ,6 PIN,R/TP ,	Y

Level	Location No.	Description	Part No.	Qty	Specification	SVC
5	U16	IC	EUSY0077602	1	SI9182DH-33-T1,MSOP-8 ,8 PIN,R/TP ,250mA CMOS LDO WIHT ERROR FLAG / 3.3V	Y
5	U18	IC	EUSY0088401	1	MC74VHC138,TSSOP ,16 PIN,R/TP ,3-TO-8 LINE DECODER	Y
5	U2	IC	EUSY0100502	1	NC7WZ08K8X,8-LEAD US8 ,8 PIN,R/TP ,UHS DUAL 2-INPUT AND GATE	Y
5	U17	IC	EUSY0111601	1	YMU762,32-PIN QFN ,32 PIN,R/TP ,MA-3 / 40 TONES / FM + WAVEFORM TABLE	Y
5	U12	IC	EUSY0116401	1	XF741979BGHH,179GHH PBGA ,179 PIN,BK ,DIGITAL BB CHIP	Y
5	U11	IC	EUSY0116501	1	PTWLR3012BGGM,100GGM PBGA ,100 PIN,BK ,ANALOG BB CHIP	Y
5	U15	IC	EUSY0119002	1	MAX4684EBC,12L UCSP ,12 PIN,R/TP ,DUAL SPDT ANALOG SWITCHES	Y
5	U13	IC	EUSY0122301	1	CIM-80S7B-T,SURFACE MOUNT ,7 PIN,R/TP ,IRDA DATA 1.3 LOW POWER TRANSCEIVER / 115.2kb/s	Y
5	U10	IC	EUSY0122401	1	S-817A18ANB-CUH-T2,SC-82AB ,4 PIN,R/TP ,CMOS LDO 1.8V OUTPUT/ 2.0 X 2.1	Y
5	SW2	IC	EUSY0129501	1	A3212ELH,SC-74A FIT ,3 PIN,R/TP ,HALL EFFECT SWITCH	Y
5	U7	IC	EUSY0144801	1	SI4201-BM,5*5 ,32 PIN,R/TP ,	Y
5	U5	IC	EUSY0144802	1	SI4133T-BM,5*5 MLP28 ,28 PIN,R/TP ,	Y
5	U6	IC	EUSY0144804	1	SI4200-BM,5*5 MLP32 ,32 PIN,R/TP ,	Y
5	U14	IC	EUSY0145401	1	TH50VPF5783AASB,P-FBGA73 ,73 PIN,R/TP ,128M FLASH 32M PSRAM / BOTTOM BOOT / CE 2 PCS	Y
5	U19	IC	EUSY0160401	1	SUY98005LT1,SOT-23 ,3 PIN,R/TP ,DC MOTOR DRIVER / INTEGERATED RELAY	Y
5	X1	VCTCXO	EXSK0000801	1	VC-TCXO-208C-13.0MHZ,13.0 MHz, PPM,10 pF,SMD ,5.0*3.2*1.5 ,	Y
5	X2	X-TAL	EXXY0004601	1	MC-146(7PF,+/-20PPM),.032768 MHz,20 PPM,7 pF,65000 ohm,SMD ,6.9*1.4*1.3 ,	Y
5	CN1	TERMINAL,PIN	MTCB0000702	1	G5400 EUASV SV,BK,7.4*2.8 4.3T Mold 2.2T 3P	Y
5	R36	THERMISTOR	SETY0001201	1	NSM4223J380H3R,NTC ,22 Kohm,SMD ,1.0*0.5 / NSM4 SERIES	Y
5	V3	VARISTOR	SEVY0000702	1	AVL14K02200,14 V,10% ,SMD ,	Y
5	V4	VARISTOR	SEVY0000702	1	AVL14K02200,14 V,10% ,SMD ,	Y
5	V5	VARISTOR	SEVY0000702	1	AVL14K02200,14 V,10% ,SMD ,	Y
5	VA1	VARISTOR	SEVY0000702	1	AVL14K02200,14 V,10% ,SMD ,	Y
5	VA2	VARISTOR	SEVY0000702	1	AVL14K02200,14 V,10% ,SMD ,	Y
5	VA3	VARISTOR	SEVY0000702	1	AVL14K02200,14 V,10% ,SMD ,	Y
5	VA4	VARISTOR	SEVY0000702	1	AVL14K02200,14 V,10% ,SMD ,	Y
5	VA7	VARISTOR	SEVY0000702	1	AVL14K02200,14 V,10% ,SMD ,	Y

Level	Location No.	Description	Part No.	Qty	Specification	SVC
5	FL1	FILTER,SEPERATOR	SFAY0001901	1	LMSP54AA-097,880/960 ,1710/1880 ,1.3 dB,1.5 dB,30 dB,25 dB,ETC ,5.4*4.0*1.8	Y
5	FB1	FILTER,BEAD,CHIP	SFBH0007101	1	BLM15AG121PN1,120 ohm,1005 ,Ferrite Bead	Y
5	FB2	FILTER,BEAD,CHIP	SFBH0007101	1	BLM15AG121PN1,120 ohm,1005 ,Ferrite Bead	Y
5	FB3	FILTER,BEAD,CHIP	SFBH0007101	1	BLM15AG121PN1,120 ohm,1005 ,Ferrite Bead	Y
5	FB4	FILTER,BEAD,CHIP	SFBH0007101	1	BLM15AG121PN1,120 ohm,1005 ,Ferrite Bead	Y
5	FB5	FILTER,BEAD,CHIP	SFBH0007101	1	BLM15AG121PN1,120 ohm,1005 ,Ferrite Bead	Y
5	FB6	FILTER,BEAD,CHIP	SFBH0007101	1	BLM15AG121PN1,120 ohm,1005 ,Ferrite Bead	Y
5	FB9	FILTER,BEAD,CHIP	SFBH0007101	1	BLM15AG121PN1,120 ohm,1005 ,Ferrite Bead	Y
5	FB10	FILTER,BEAD,CHIP	SFBH0007101	1	BLM15AG121PN1,120 ohm,1005 ,Ferrite Bead	Y
5	FB11	FILTER,BEAD,CHIP	SFBH0007101	1	BLM15AG121PN1,120 ohm,1005 ,Ferrite Bead	Y
5	FB12	FILTER,BEAD,CHIP	SFBH0007101	1	BLM15AG121PN1,120 ohm,1005 ,Ferrite Bead	Y
5	FB13	FILTER,BEAD,CHIP	SFBH0007101	1	BLM15AG121PN1,120 ohm,1005 ,Ferrite Bead	Y
5	FB14	FILTER,BEAD,CHIP	SFBH0007101	1	BLM15AG121PN1,120 ohm,1005 ,Ferrite Bead	Y
5	FB15	FILTER,BEAD,CHIP	SFBH0007101	1	BLM15AG121PN1,120 ohm,1005 ,Ferrite Bead	Y
5	FB16	FILTER,BEAD,CHIP	SFBH0007101	1	BLM15AG121PN1,120 ohm,1005 ,Ferrite Bead	Y
5	FB17	FILTER,BEAD,CHIP	SFBH0007101	1	BLM15AG121PN1,120 ohm,1005 ,Ferrite Bead	Y
5	FB18	FILTER,BEAD,CHIP	SFBH0007101	1	BLM15AG121PN1,120 ohm,1005 ,Ferrite Bead	Y
5	FB19	FILTER,BEAD,CHIP	SFBH0007101	1	BLM15AG121PN1,120 ohm,1005 ,Ferrite Bead	Y
5	FB20	FILTER,BEAD,CHIP	SFBH0007101	1	BLM15AG121PN1,120 ohm,1005 ,Ferrite Bead	Y
5	FB21	FILTER,BEAD,CHIP	SFBH0007101	1	BLM15AG121PN1,120 ohm,1005 ,Ferrite Bead	Y
5	FB22	FILTER,BEAD,CHIP	SFBH0007101	1	BLM15AG121PN1,120 ohm,1005 ,Ferrite Bead	Y
5	FB23	FILTER,BEAD,CHIP	SFBH0007101	1	BLM15AG121PN1,120 ohm,1005 ,Ferrite Bead	Y
5	FB24	FILTER,BEAD,CHIP	SFBH0007101	1	BLM15AG121PN1,120 ohm,1005 ,Ferrite Bead	Y
5	FB25	FILTER,BEAD,CHIP	SFBH0007101	1	BLM15AG121PN1,120 ohm,1005 ,Ferrite Bead	Y
5	FB26	FILTER,BEAD,CHIP	SFBH0007101	1	BLM15AG121PN1,120 ohm,1005 ,Ferrite Bead	Y
5	FB27	FILTER,BEAD,CHIP	SFBH0007101	1	BLM15AG121PN1,120 ohm,1005 ,Ferrite Bead	Y
5	L8	FILTER,BEAD,CHIP	SFBH0007102	1	BLM15AG100PN1,10 ohm,1005 ,Ferrite Bead	Y
5	L9	FILTER,BEAD,CHIP	SFBH0007102	1	BLM15AG100PN1,10 ohm,1005 ,Ferrite Bead	Y
5	FL2	FILTER,SAW	SFSY0012202	1	SAFSD942MFM0T00,942.5 MHz,2.0*2.5*1.0 ,SMD ,	Y
5	FL3	FILTER,SAW	SFSY0012302	1	SAFSD1G84FA0T00R00,1842.5 MHz,2.0*2.5*1.0 ,SMD ,	Y
5	U4	PAM	SMPY0004001	1	RF3133,35 dBm,55 %,2 A,-50 dBc,25 dB,10.0 * 7.0 * 1.4 ,SMD ,	Y
5	SPFY00	PCB,MAIN	SPFY0046101	1	G7030 EUASV,MAIN,1.1,FR-4 ,1 mm,MULTI-8 ,Revision 1.1	N